Using Quickfilter IC's in an Environment with Multiple SPI Devices

1) Introduction

All Quickfilter filter IC's (QF1D512, QF1Da512, and QF4A512) are designed to interface directly with the serial peripheral interface (SPI) bus of microcontrollers and Digital Signal Processors. The SPI bus is used in Configuration Mode to initialize and configure each device, as well as in Data Mode during normal operation of the part.

In Data Mode, the QF1D filters accept a variety of interface protocols -- I2S, Synchronous Serial, SPI Normal, and SPI Continuous. For the QF4A, Data Mode (also known as Run Mode), is a conventional SPI protocol used to send the filtered data out of the QF4A512 via the SDO pin, with new data signaled by the Data Ready pin, DRDY, and clocked by an SPI master via SCL.

When used alone on a dedicated SPI bus, these devices can be tied directly to the bus without the use of any additional circuitry. In an environment in which two or more SPI slaves reside, the use of any of the SPI protocols (except I2S and Synchronous Serial) require additional logic – a simple gating for the data clock. This application note illustrates the use of that logic.

For more detailed information on this and all other aspects of the QF1D and QF4A filters, refer to the appropriate data sheets available on the Quickfilter website, www.quickfiltertech.com.

2) Data Mode

The QF1D family supports I2S or SPI and is designed to interface directly with a variety of ADC converters using one of these four modes (See Figure 2):

1. I2S Mode

   A word select line (**WS** on the **dCS** input) indicates which of two time-division multiplexed data channels is being transmitted. The channels are transmitted alternately on the data line (**SD** on the **dSDI** input) and are synchronized by a clock line (**SCK** on the **dSCK** input).

2. SPI Normal Mode
   The data is framed by the **dCS** input signal

3. SPI Continuous Mode
   Once **dCS** is active, data is output corresponding to clock bursts on the **dSCK** input.

4. SPI Synchronous Serial Mode

   dCS is used as a trigger to indicate the start of each new sample period. **dSCK** runs continuously, filtered data is output on the next *n* cycles of **dSCK** according to the programmed word length.

The data interface utilizes the **dSDI** (**SD** for I2S), **dSDO** (**SD** for I2S), **dCS** (**WS** for I2S) and **dSCK** (**SCK** for I2S) pins. **dSDI** is the input serial data, and **dSDO** is the output serial data (if **FILT_EN** = 1). **dSCK** is the input data clock and **dCS** is the framing signal for the input data.

In I2S Mode, Synchronous Serial Mode, and SPI Continuous Mode the data clock, dSCK, can, by definition, be present at either state of the chip select signal, dCS.

In either SPI mode, data should be presented to the part only when dCS is active. In other words, the data clock, dSCK, should not clock unless dCS is active. In a design in which the QF1D parts are the only device on the SPI bus, SPI Normal mode or SPI Continuous mode can be implemented identically to the other modes – a direct connection for all of the control signals. When multiple SPI slave devices exist on the same SPI bus and an SPI Mode is to be used, then the QF1D's dSCK input must be protected from any dSCK state changes while dCS is inactive. This requires a simple gate as illustrated in Figures 3 and 4.

Similarly, when using the QF4A with other SPI slave devices on the same bus, the QF4A's chip select pin, /CS, should be gated in the same manner.

Waveforms showing SCLK and a gated SCLK to allow Data transfers to work in SPI Normal Mode
using a standard SPI Bus (not one that stops clocks when CS_N is deasserted).
Data is sampled on the rising edge of SCLK and driven on the falling edge of SCLK

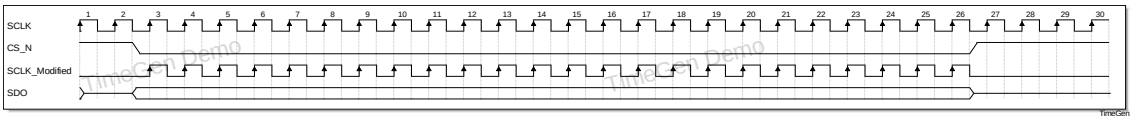

Figure 1: Gated SCLK Waveforms

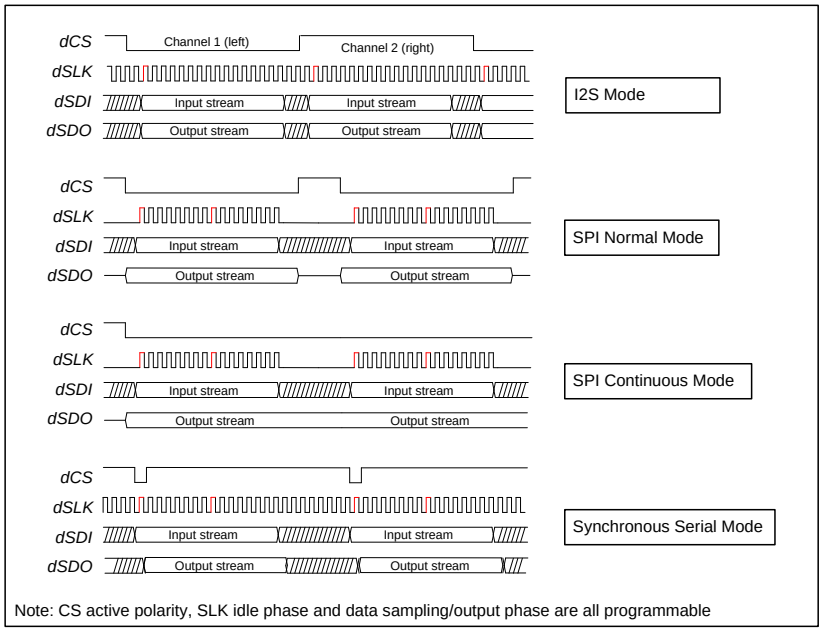

Figure 2: Data Interface Modes

3) Schematics

Here are two examples illustrating a simple method for gating the SPI clock.

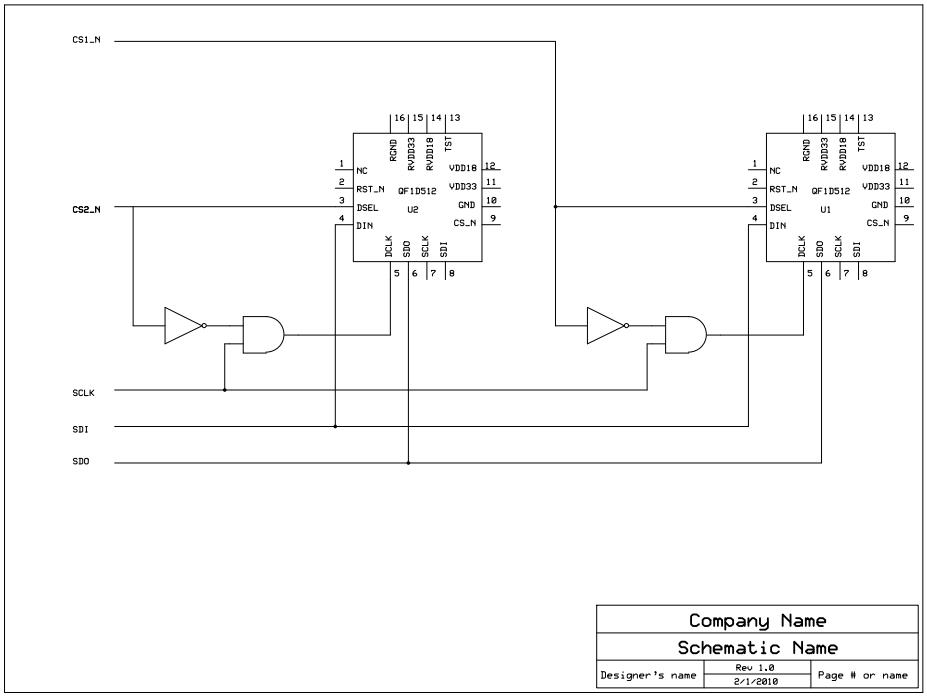

Figure 3: Separate Chip Selects using SPI Normal Mode

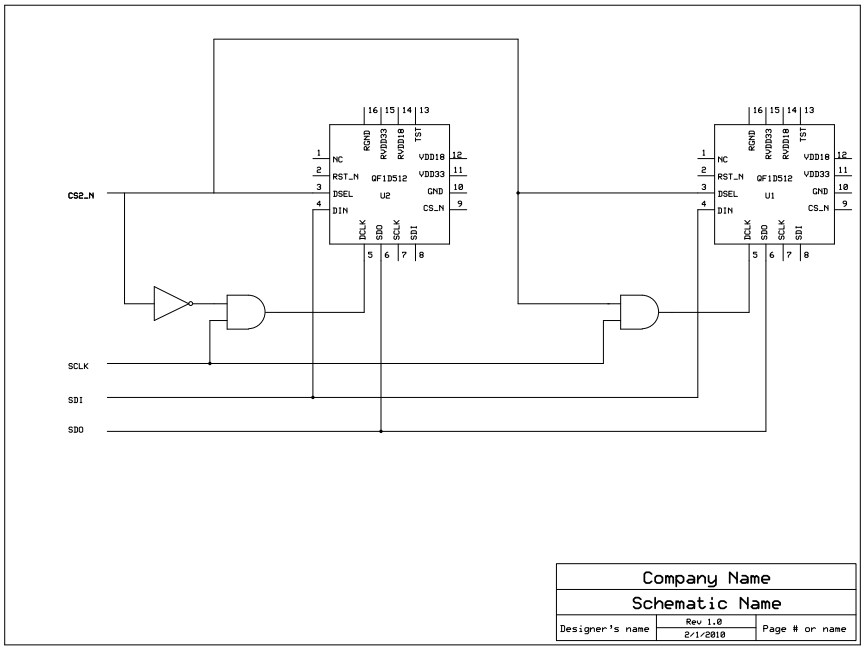

Figure 3: Shared Chip Select using SPI Normal Mode

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