Synchronized Sampling Using Multiple QF4A512 Programmable Signal Converters

1) Introduction

A single QF4A512 Programmable Signal Converter chip [1] can sample 4 analog signals simultaneously. However, some applications sample more than 4 channels using multiple QF4A512 chips, as described in Quickfilter App Note QFAN005 [2]. Some systems additionally require that the samples across multiple chips be tightly synchronized. This App Note describes a simple additional procedure to synchronize multiple QF4A512 devices so that all analog signals are sampled at the same moment and all DRDY signals assert synchronously.

2) Functional Description

An example circuit is shown in Figure 1. With a synchronized set of QF4A512 devices, one DRDY signal will represent data ready for all the devices, so only one GPIO is needed, for example, for the DRDY handshake.

Connection Diagram For Synchronous Sampling

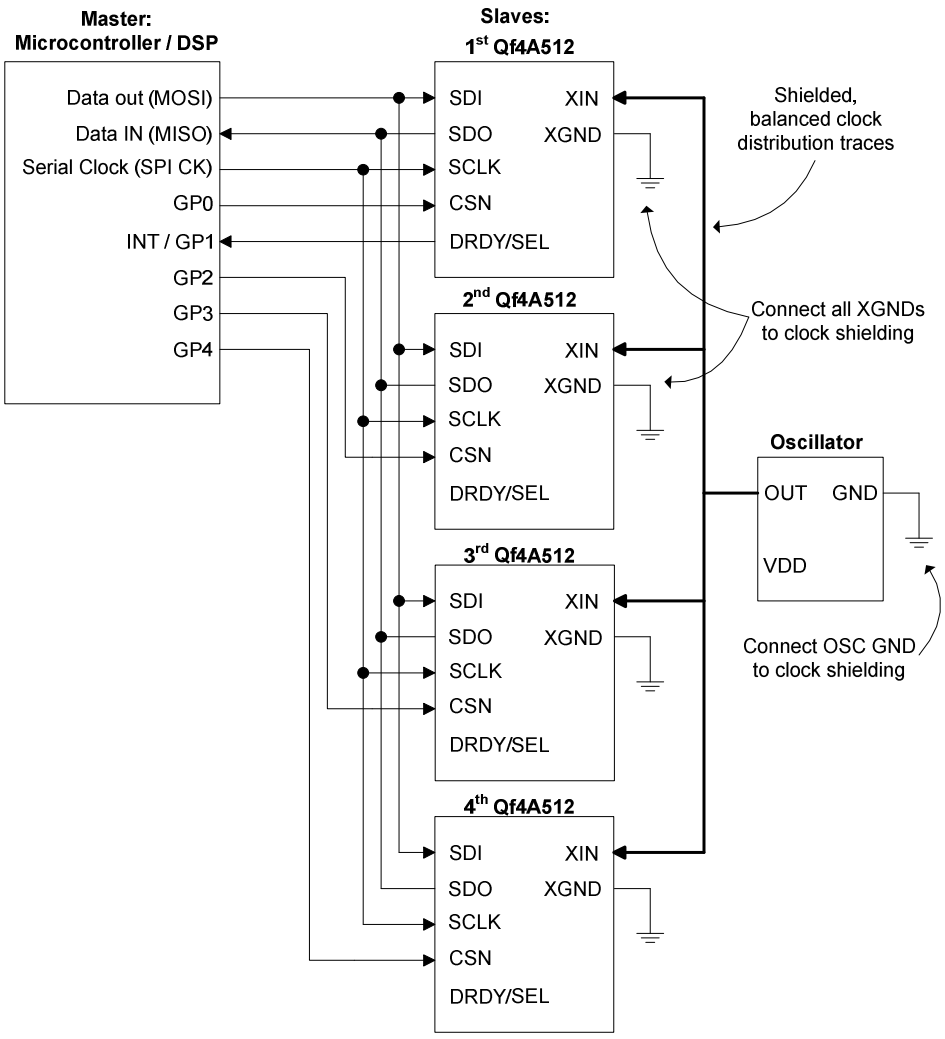

Figure 1

The two main design steps to synchronize QF4A512 device sampling are generating a synchronous XIN clock, and broadcasting a sequence of SPI commands to all devices to simultaneously reset the internal sampling logic of all devices.

1. **Generating a synchronous XIN clock.**

   For a single chip QF4A512 application, as shown in the datasheet [1], the XIN/XOUT pin pair are normally connected to an external crystal with the QF4A512 internal oscillator activated to generate a clock reference (e.g. 20 MHz) for all sampling and computation circuits inside the QF4A512 device. However, to operate multiple QF4A512's in a synchronized sampling mode, the clock reference for all devices must come from the same source. For example, the example circuit Figure 1 shows a discrete oscillator supplying a clock reference to the XIN pins of multiple QF4A512's.

   Besides generating a single source distributed to all QF4A512's in a system, care must be take to preserve the signal integrity of the clock as it is distributed from the source (eg external discrete oscillator) to each QF4A512. The full topic of system clock distribution is beyond the scope of this app note. Also the specific requirements differ for any given system. The reader is directed to reference [3] for more information on clock distribution to include techniques for buffering, shielding, impedance matching, and noise isolation.

2. **Simultaneous reset of QF4A512 sampling logic.**

   This section details the SPI command sequence necessary to synchronize the sampling of multiple QF4A512 devices clocked by the same XIN clock.

   Assumptions:
   - All QF4A512 device XIN pins are clocked by a single, well-conditioned clock source
   - All QF4A512 SPI buses are operated in broadcast mode for chip configuration. All CSN pins are activated simultaneously, so the SDO pins are connected to separate buses.
   - All QF4A512 devices have the same configuration. This will happen with no additional effort with the devices are in broadcast mode.

   Programming sequence (broadcast to all QF4A512 devices):
   1. Enable the ram clocks (ram_run_mode : addr 0x15 SPI_CONTROL, bit 0, set to 1)
   2. Cycle the clock divider reset (pcg_srst : addr 0x26 GLBL_SRST, bit 0, cycle to 1 then back to 0)
   3. Cycle the analog receiver reset (arec_srst : addr 0x26 GLBL_SRST, bit 3, cycle to 1 then back to 0)
   4. Cycle the digital data path reset (ch*n*_srst : addr 0x03 GLBL_CH_CTRL, bits 0-3, cycle to 0xf then back to 0)

   At the end of the programming sequence, all QF4A512 devices will be processing their respective data paths synchronously. The DRDY pins on all devices will assert simultaneously, signifying that new data is ready from each device at the same time.

The clock distribution and synchronizing sequence has been demonstrated in the lab using 2 QF4A512-DK development kits and a Citizen CMX-209 20 MHz oscillator.

3) References

[1] "4-Channel Programmable Signal Converter". QF4A512 Datasheet. Quickfilter Technologies. www.quickfiltertech.com.

[2] "Multiple Chip Configuration." App Note QFAN005. Quickfilter Technologies. www.quickfiltertech.com

[3] Noise Reduction Techniques in Electronic Systems, 2nd Edition by Henry Ott. Wiley-Interscience, 1988.

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