DC Calibration of the QF4A512 Programmable Signal Converter

1) Introduction

This Application Note describes the DC calibration features of the QF4A512 which can be used not only to remove sources of measurement errors in the device itself, but also variations in the external system front end components.

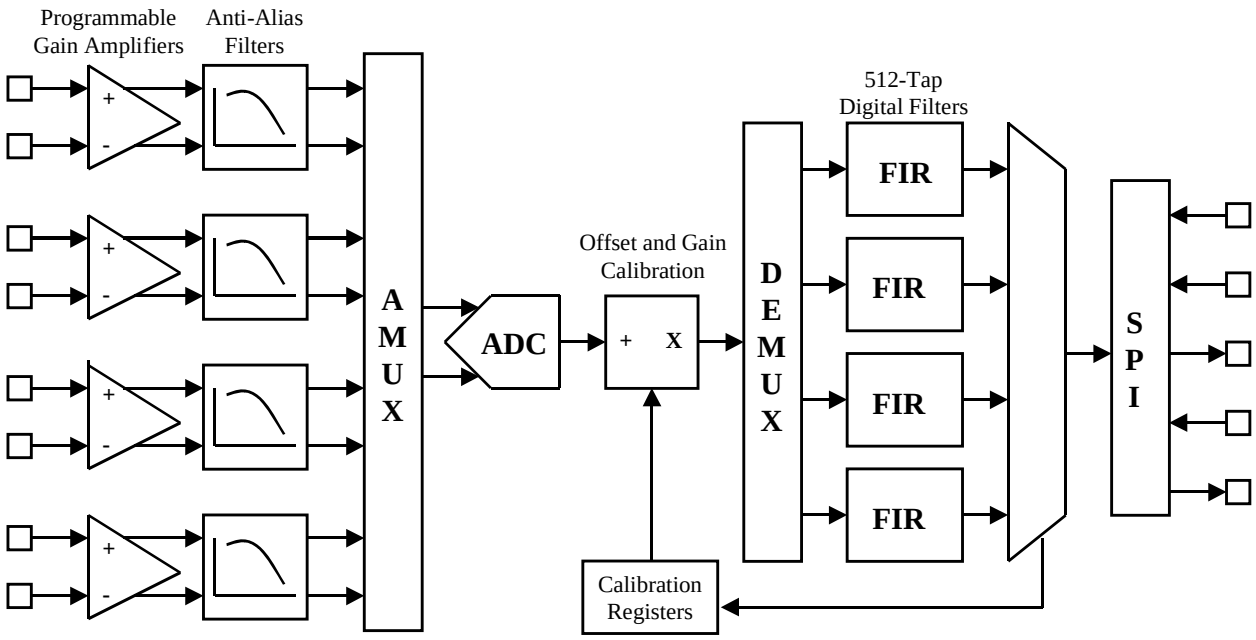
This application note describes the following:

- Overview.
- DC offset calibration.
- DC gain calibration.
- Example Use of a Extended Calibration Sequence.
- Calibration of QF4A512 Error Sources

2) Overview

Figure 1 shows the block diagram of the QF4A512.

Figure 1 – QF4A512 Block Diagram



Included in the device are calibration registers, which provide an offset and gain adjustment on a per channel basis to the samples after the ADC. The QF4A512 supports a calibration mode, which makes the calibration a simple process. The user sets the device for calibration, selects the desired output level, and then inputs the calibration signal. The QF4A512 will then take the measurement, determine what the calibration value needs to be, and then loads this value in the calibration registers (**CAL_x_OFF** and **CAL_x_GAIN**).

To make sure the ADC inside the QF4A512 is operating across the proper voltage range, the proper series resistors and gain settings for the PGA need to be used. Table 1 shows the recommended input series resistors and PGA gain settings for various ranges of voltage inputs.

Desired DC Input Voltage	Series resistors R1-R8	PGA setting
-0.25V +0.25V	10K	x8
-0.5 to +0.5V	10K	x4
-1V to 1V	10K	x2
-2V to 2V	10K	x1
-3V to 3V	20K	x1
-3.3V to 3.3V	23K	x1
-5V to 5V	40K	x1
-10V to 10V	90K	x1
-12V to 12V	110K	x1
-15V to 15V	140K	x1
-20V to 20V	190K	x1
-24V to 24V	230K	x1
-28V to 28V	270K	x1

Table 1

3) DC Offset Calibration

Ideally the maximum input voltage to the QF4A512 should correspond to a full-scale reading from the ADC. If the input signal is too low to achieve this, then the PGA gain can be adjusted to provide a larger signal to the ADC.

Design Note

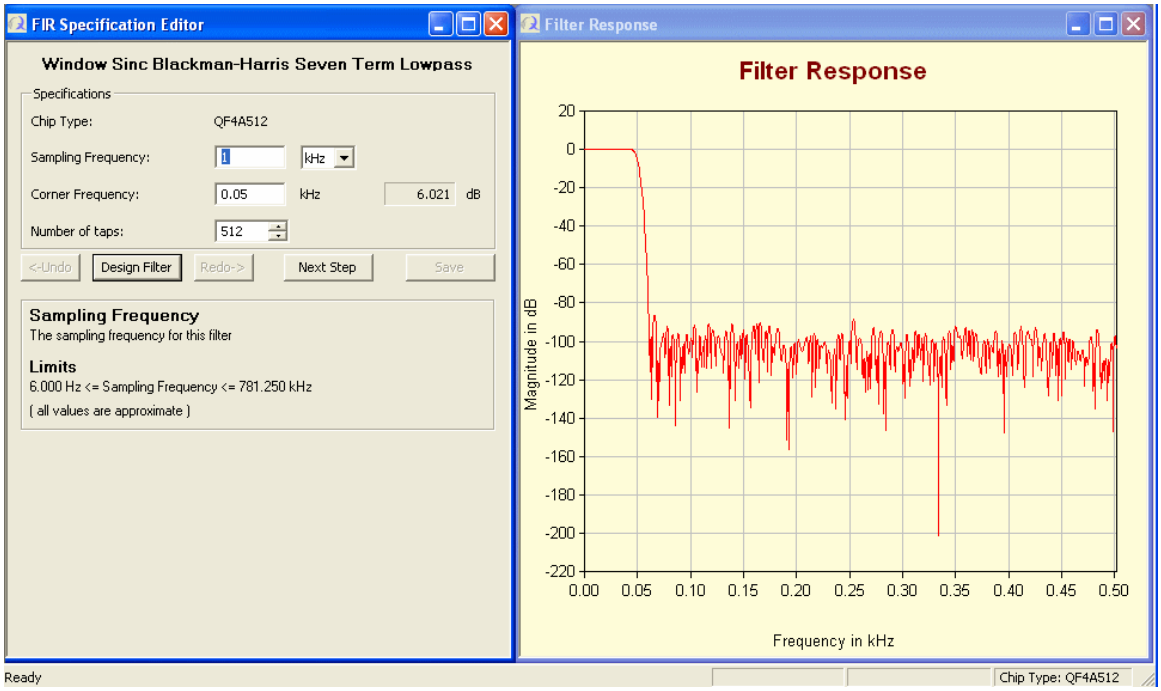
The QF4A512 software enables a chopper circuit for designs using a sample rate of 200K or less. When the chopper is enabled, DC offset is reduced, running calibration will further improve the offset measurement. The chopper will be enabled automatically by the software for sample rates below 200KHz. The choppers main purpose is to eliminate 1/f noise at lower frequencies.

For calibration, a low pass filter should be selected. Minimal ripple in the passband will give better results. A sample filter has been designed, using a 50 Hz bandwidth sampled at 1 KHz. All 512 taps have been used for best performance.

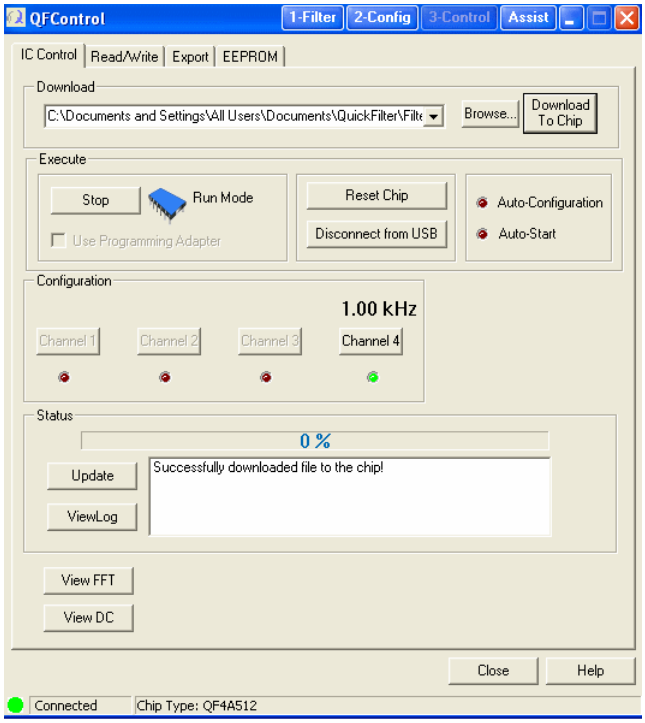
Step 1: Connect the input signal(s) to 0 Volts.

Step 2: Using the QuickFilter software, run “File > Open Filter >”. Select the lpf.qff file.

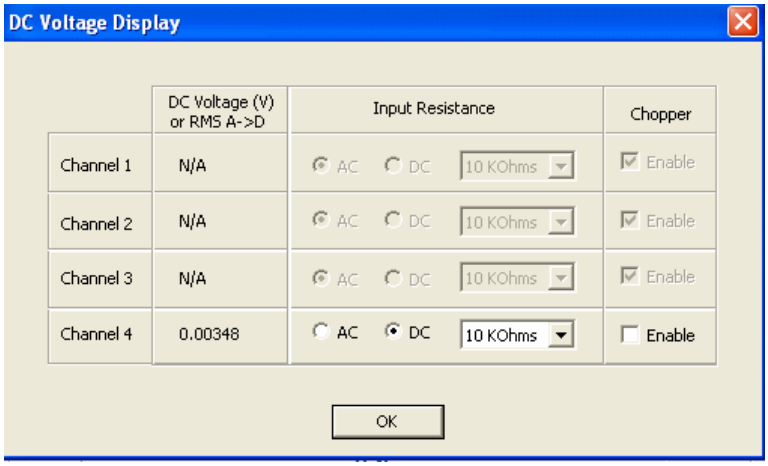
Step 3: Select “Design Filter” and Save.



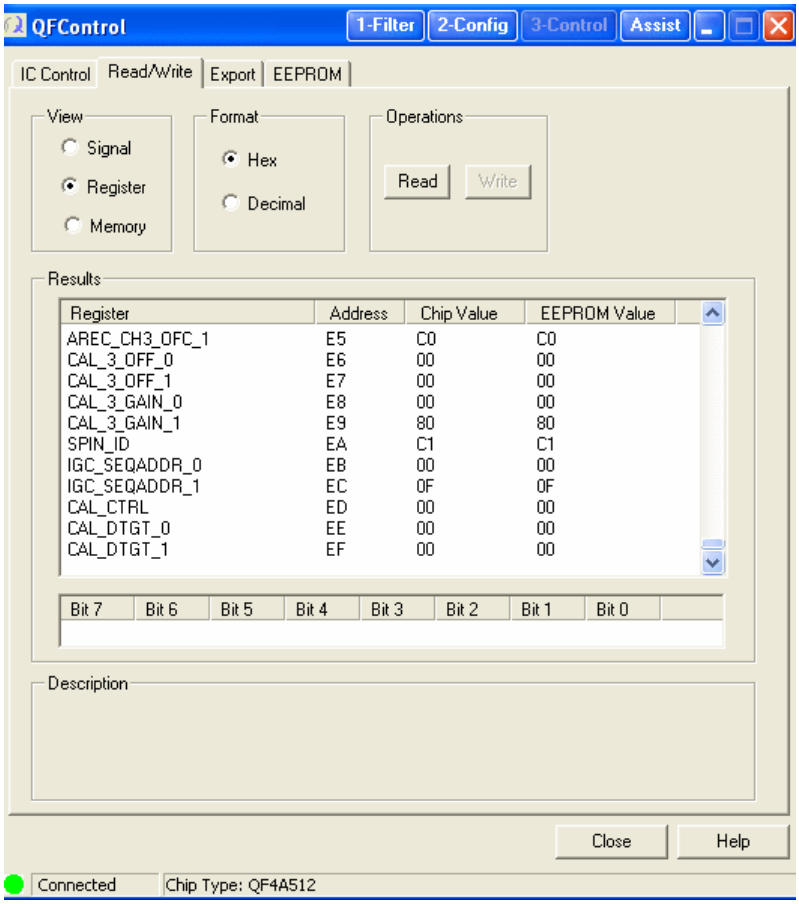
Step 4: Select “Next Step”. Highlight the channel desired and hit “Load”. Select the filter file “lpf.qff”. Hit “Configure” and “Save”. Select the “Control” tab at the top of the page.



Step 5: Select the “Download to Chip” button. Select the “View DC” button. Select DC. If your sampling frequency is over 200KHz, deselect the “Chopper Enable”. Close this window..



Step 6: Select the “Read/Write” tab. Select the “Register” radio button. Move the slider bar down so that the **CAL_CTRL** register is visible (address 0xED).



Step 6: Make sure the **CAL_DTGT_0/1** registers are set to 00. This sets the value which the QF4A512 will correct the data to. Make sure the **CAL_x_OFF_0/1** registers are set to 00. This resets the offset value to the default value, with no offset added to the signal. In the **CAL_CTRL** register of the QF4A512, set bits 0 & 1 to select the channel being calibrated. Set bit 2 to '0' to select the offset calibration. Set bit 3 to '1' to start the calibration. Make sure bit 4 is set to '0', this bit sets the soft reset for the calibration circuit if set to '1'. Writing these values to this register initiates the calibration.

Design Note

All of the registers that have more than one address value (for example CAL_DTGT_0 & CAL_DTGT_1), need to have the lower register (CAL_DTGT_0) written first, then the upper one. The value is updated after the upper register is written.

Step 7: If you select READ button on the Read/Write tab, you will now see the calculated offset calibration value in the **CAL_x_OFF_0/1** registers.

Step 8: Return to the "View DC" window to see the effects of the calibration.

4) Gain Calibration

Gain is calibrated in the QF4A512 by setting up a reference voltage coming into the part, setting the corresponding output value of the part and then performing calibration. The voltage will depend on the input series resistance and the PGA settings. **Table 1** shows the calibration voltages when the **CAL_x_DTGT_0/1** registers are set to 00h and 30h respectively.

Table 2: Calibration Voltages

Desired DC Input Voltage	Series resistors R1-R8	PGA setting	Calibration Voltage
-0.1V +0.25V	10K	x8	94mV
-0.25V to +0.5V	10K	x4	187mV
-0.5V to 1V	10K	x2	0.375V
-1V to 2V	10K	x1	0.75V
-1.5V to 3V	20K	x1	1.125V
-2V to 3.3V	23K	x1	1.245V
-5V to 5V	40K	x1	1.5V
-10V to 10V	90K	x1	3.75V
-12V to 12V	110K	x1	4.5V
-12V to 12V	230K	x2	2.25V
-15V to 15V	140K	x1	5.625V
-20V to 20V	190K	x1	7.5V
-24V to 24V	230K	x1	9V
-28V to 28V	270K	x1	10.5V

Design Note

The software calculates the DC voltage based on the Input Resistance selected on the DC Voltage Display. If the actual input resistance differs from the selection on the display, the calculated voltage will not match the input voltage see table 3.

Step 1: Connect the reference voltage to the input of the signal path. Select the value from Table 1 or calculate using the following formula: $V_{REF} = V_{ADC} * (R_{SERIES} + 10K) / 10K$ where $V_{ADC} = 0.375$ V.

Design Note

Different calibration target voltages can be used. Here is a list of settings for the **CAL_DTGT_0/1** registers versus the voltage seen at the A/D converter:

V_{ADC}	CAL_DTGT_0	CAL_DTGT_1
0.375 V	00h	30h
0.50 V	00h	40h
0.75 V	00h	60h

The following table shows some common reference voltages "VREF" which could be used for calibration coming into the series resistor into the QF4A512 and what the corresponding CAL_DTGT_0/1 value should be.

VREF (DC)	Input series resistors	Decimal	Target Value	CAL_DTGT_0 HEX	CAL_DTGT_1 HEX
0.375V	0	12288	3000h	00	30
0.75V	10K	12288	3000h	00	30
1.2V	0	Out of range			
1.2V	10K	19660	4CCCh	CC	4C
1.2V	20K	13107	3333h	33	33
1.2V	23.2K	11843	2E43h	43	2E
1.2V	40K	7864	1EB8h	B8	1E
1.2V	91K	Resolution too low for accurate calibration			
1.8V	10K	29491	7333h	33	73
2.5V	10K	Out of range			
2.5V	20K	27306	6AAAh	AA	6A
2.5V	23.2K	24674	6062h	62	60
2.5V	40K	16384	4000h	00	40
2.5V	91K	8110	1FAEh	AE	1F
2.5V	110K	6826	1AAAh	AA	1A
2.5V	140K	5461	1555h	55	15
2.5V	191K	Resolution too low for accurate calibration			
4.096V	20K	Out of range			
4.096V	40K	26843	68DBh	DB	68
4.096V	91K	13288	33E8h	E8	33
4.096V	110K	11184	2BB0h	B0	2B
4.096V	140K	8947	22F3h	F3	22
4.096V	191K	6677	1A15h	15	1A
4.096V	232K	5546	15AAh	AA	15
4.096V	270K	4793	12B9h	B9	12

Table 3

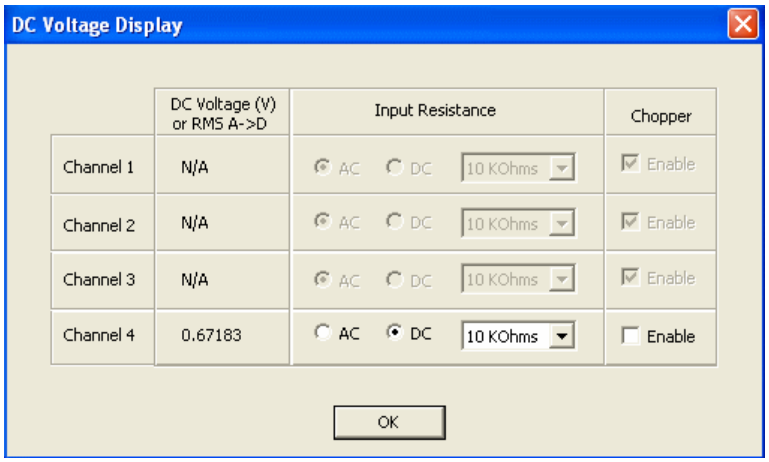
The formula for finding the target calibration number is:

X= (V*12,288) / 0.375 = decimal value not to exceed (32768)

Convert X to hexadecimal and store in CAL_DTGT_0, write the least significant byte first. Then write CAL_DTGT_1, write the most significant byte last. Then read it back twice to show that the value is now correct.

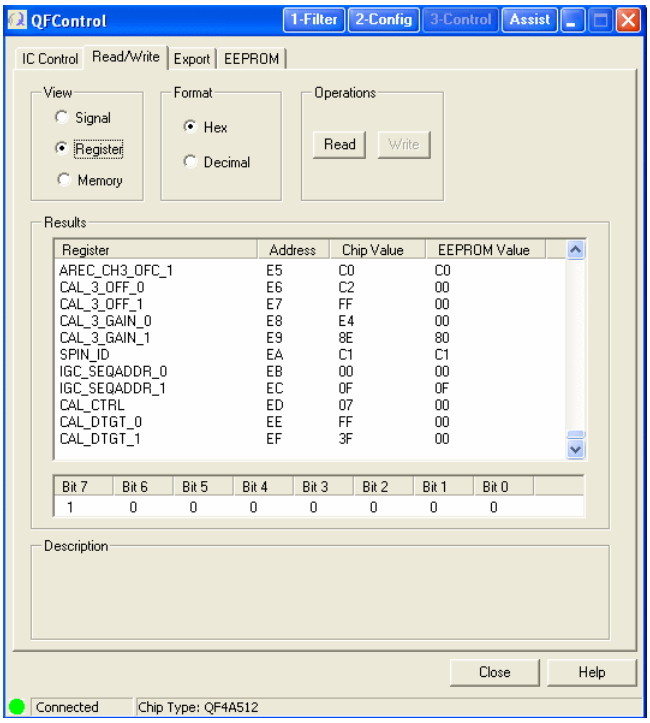
Where, x= calibration number in decimal, must convert to hexadecimal.
V= voltage at the QF4A512 input channel after the resistor divide.
(V is calculated by the series input resistor divided by a 10K resistor to ground internally.)

Step 2: Go to the "View DC" window and record the indicated voltage.



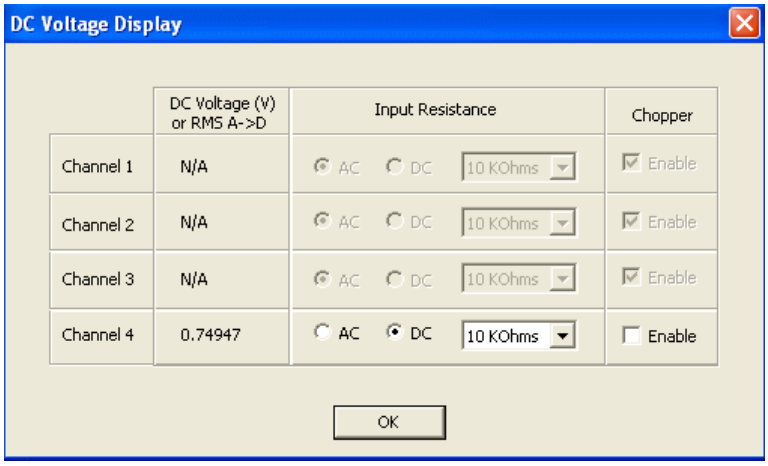
Step 3: Select the "Read/Write" tab. Select the "Register" radio button. Move the slider bar down so that the **CAL_CTRL** register is visible (address 0xED). Make sure the **CAL_DTGT_0** registers is set to 00. Make sure **CAL_DTGT_1** is set to 30 or other value from the above table. The **CAL_DTGT_0/1** registers hold the target output value from the ADC for the applied reference voltage.

Step 4: Make sure the **CAL_x_GAIN_0** register is set to 00. Make sure that **CAL_x_GAIN_1** register is set to 80. These have to be written in order. This sets the gain to the default value, which is unity gain. In the **CAL_CTRL** register of the QF4A512, set bits 0 & 1 to select the channel being calibrated. Set bit 2 to '1' to select the gain calibration. Set bit 3 to '1' to start the calibration. Make sure bit 4 is set to '0', this bit sets the soft reset for the calibration circuit if set to '1'. Writing these values to this register initiates the calibration.

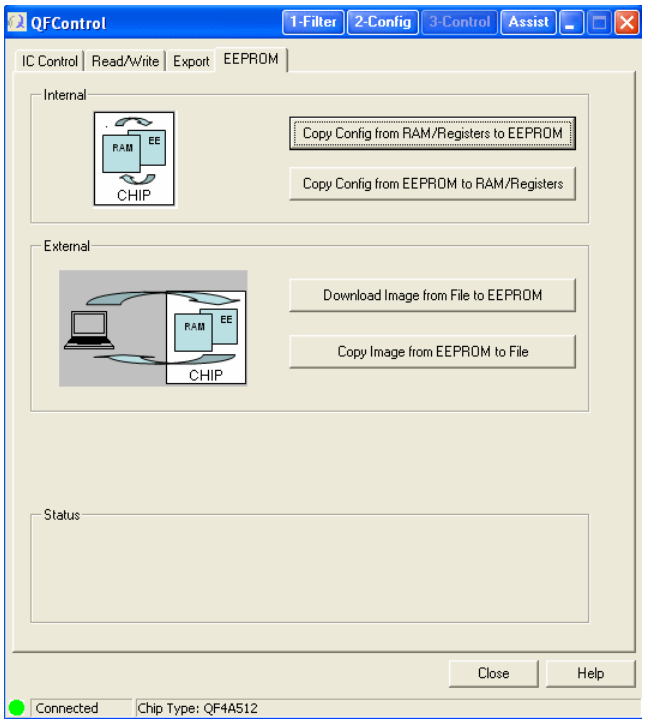


Step 5: If you select READ button on the Read/Write tab, you will now see the calculated gain calibration value in the **CAL_x_GAIN_0/1** registers.

Step 6: Return to the “View DC” window to see the effects of the calibration.



Additionally, the calibration values determined in this process can be written into the EEPROM registers of the QF4A512. The device can be configured to load these values upon reset



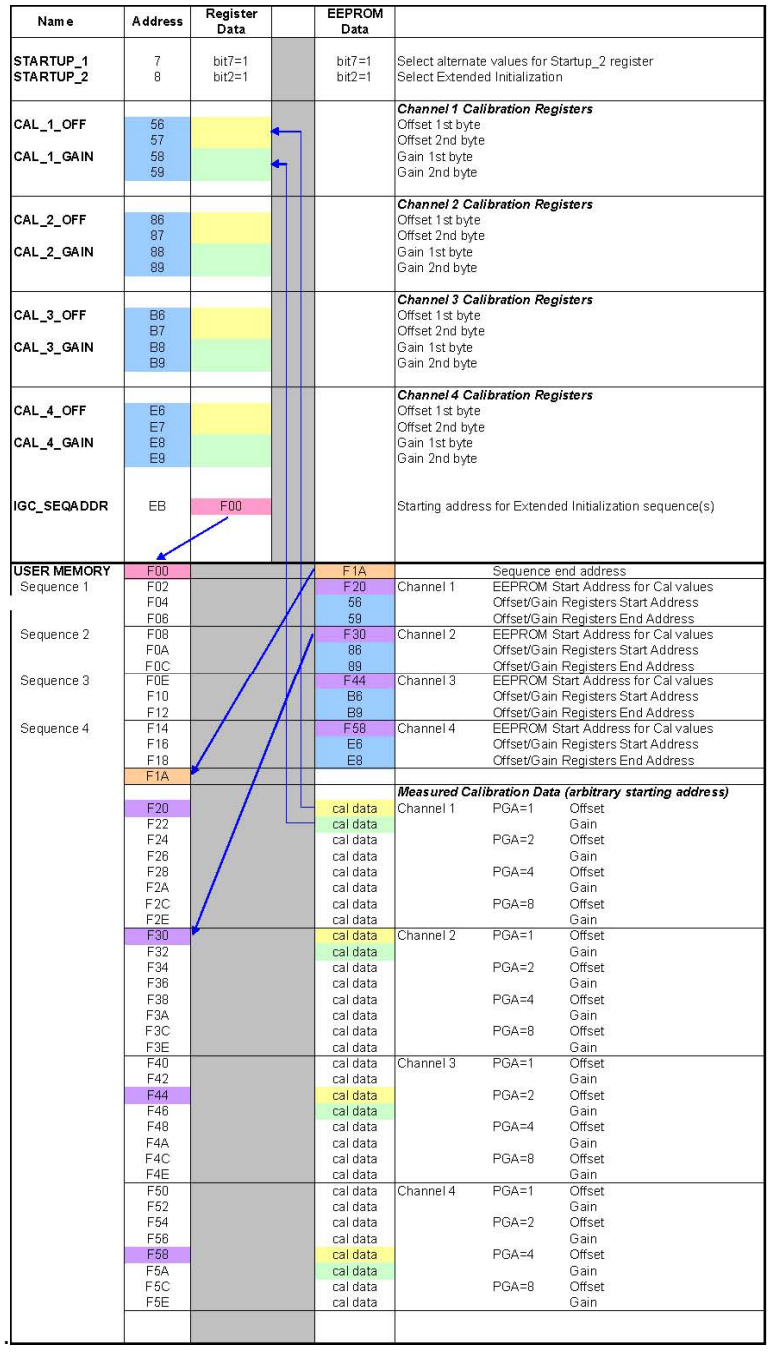
5) Example Use of an Extended Initialization Sequence

The optimum values for the gain and offset calibration will vary from channel to channel and also with PGA gain settings. In the following example we will show how calibration values can be stored for all possible configurations and then loading the appropriate values after a device reset or power on. It is also possible to have multiple values per channel to allow for different calibration points over temperature, voltage levels, or whatever parameter that might cause the values to change.

Example Configuration

Channel 1 = PGA gain x1
Channel 2 = PGA gain x1
Channel 3 = PGA gain x2
Channel 4 = PGA gain x4

The relevant registers and the memory map shown in Figure 2. Note how sequence 1 points to the correct locations for channel 1, sequence 2 for channel 2, and so on.



Name	Address	Register Data		EEPROM Data			
STARTUP_1	7	bit7=1		bit7=1	Select alternate values for Startup_2 register		
STARTUP_2	8	bit2=1		bit2=1	Select Extended Initialization		
					Channel 1 Calibration Registers		
CAL_1_OFF	56				Offset 1st byte		
	57				Offset 2nd byte		
CAL_1_GAIN	58				Gain 1st byte		
	59				Gain 2nd byte		
					Channel 2 Calibration Registers		
CAL_2_OFF	86				Offset 1st byte		
	87				Offset 2nd byte		
CAL_2_GAIN	88				Gain 1st byte		
	89				Gain 2nd byte		
					Channel 3 Calibration Registers		
CAL_3_OFF	B6				Offset 1st byte		
	B7				Offset 2nd byte		
CAL_3_GAIN	B8				Gain 1st byte		
	B9				Gain 2nd byte		
					Channel 4 Calibration Registers		
CAL_4_OFF	E6				Offset 1st byte		
	E7				Offset 2nd byte		
CAL_4_GAIN	E8				Gain 1st byte		
	E9				Gain 2nd byte		
IGC_SEQADDR	EB	F00			Starting address for Extended Initialization sequence(s)		
USER MEMORY	F00			F1A		Sequence end address	
Sequence 1	F02			F20	Channel 1	EEPROM Start Address for Cal values	
	F04			56		Offset/Gain Registers Start Address	
	F06			59		Offset/Gain Registers End Address	
Sequence 2	F08			F30	Channel 2	EEPROM Start Address for Cal values	
	F0A			86		Offset/Gain Registers Start Address	
	F0C			89		Offset/Gain Registers End Address	
Sequence 3	F0E			F44	Channel 3	EEPROM Start Address for Cal values	
	F10			B6		Offset/Gain Registers Start Address	
	F12			B9		Offset/Gain Registers End Address	
Sequence 4	F14			F58	Channel 4	EEPROM Start Address for Cal values	
	F16			E6		Offset/Gain Registers Start Address	
	F18			E8		Offset/Gain Registers End Address	
	F1A						
					Measured Calibration Data (arbitrary starting address)		
	F20			cal data	Channel 1	PGA=1	Offset
	F22			cal data			Gain
	F24			cal data		PGA=2	Offset
	F26			cal data			Gain
	F28			cal data		PGA=4	Offset
	F2A			cal data			Gain
	F2C			cal data		PGA=8	Offset
	F2E			cal data			Gain
	F30			cal data	Channel 2	PGA=1	Offset
	F32			cal data			Gain
	F34			cal data		PGA=2	Offset
	F36			cal data			Gain
	F38			cal data		PGA=4	Offset
	F3A			cal data			Gain
	F3C			cal data		PGA=8	Offset
	F3E			cal data			Gain
	F40			cal data	Channel 3	PGA=1	Offset
	F42			cal data			Gain
	F44			cal data		PGA=2	Offset
	F46			cal data			Gain
	F48			cal data		PGA=4	Offset
	F4A			cal data			Gain
	F4C			cal data		PGA=8	Offset
	F4E			cal data			Gain
	F50			cal data	Channel 4	PGA=1	Offset
	F52			cal data			Gain
	F54			cal data		PGA=2	Offset
	F56			cal data			Gain
	F58			cal data		PGA=4	Offset
	F5A			cal data			Gain
	F5C			cal data		PGA=8	Offset
	F5E			cal data			Gain

Figure 2

6) Calibration of QF4A512 Error Sources

Many of the sources of measurement errors can be compensated with the gain and offset calibration of the QF4A512. One of the error sources of the QF4A512 is the inaccuracy of the internal voltage reference under different load conditions. Another source is variation of the internal load resistance from the 10K ideal value. Both of these error sources will cause gain and offset errors in DC measurements. The calibration capability of the QF4A512 can be used to remove these errors in the measurement.

7) Summary

Digital calibration can be used to correct offset and gain errors seen in the device and the input voltage divider network. By inputting in a known reference voltage and programming the expected value, the calibration function in the QF4A512 can calibrate for gain and offset, getting improved DC performance.

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