Using an External Clock to Drive the QF4A512 Programmable Signal Converter

1) Introduction

This Application Note describes using an external clock source to run Quickfilter's QF4A512 Programmable Signal Converter. The advantage of using an existing clock source means not having to have an external 20 MHz crystal attached to Pins 22 and 23 saving cost and real estate. The external clock source can range from 5 MHz to 300 MHz depending on the filter design's sample rate.

This application note covers the following:

- Physical connection to the development board and design considerations.
- Range of usable external clock frequencies.
- Using Quickfilter's software to correctly utilize the external clock source.

2) Development board external clock source connection.

Since the crystal is lightly loaded, and external driving clock source can directly run the internal oscillator.
You do not need to remove the 1 Meg resistor, crystal or 18 pF loading capacitors from the development board.

Quickfilter Development Board External Clock connection

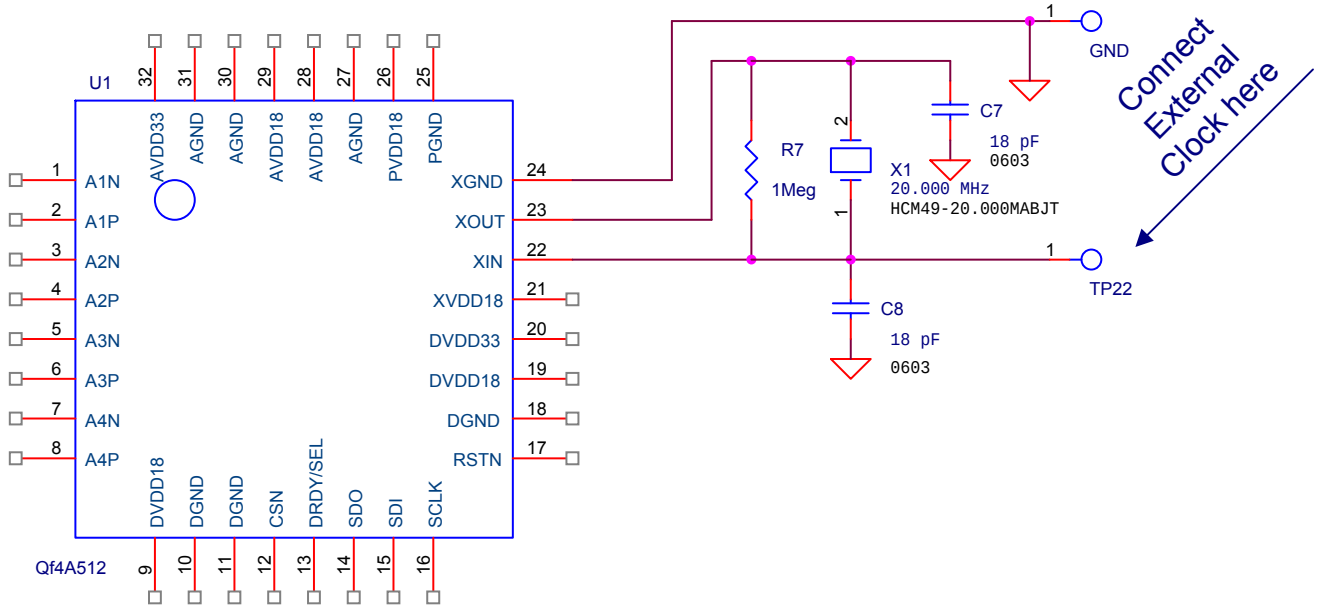


Figure 1

3) Designing using an external clock source.

When designing using an external clock source the external crystal X1 and it's support components can be removed saving cost and real estate. Note: you can also use a different crystal other than 20 MHz.

Designer's note – The allowable input range is 5 MHz to 200 MHz.

The clock input on Pin 22 to the phase lock loop is a 1.8V level. The clock is a logic level which swings from zero to 1.8V. The actual range is a minimum 0.4V to the upper level threshold (1.62 to 1.98 Volts). The clock can be a sine wave, or square wave.

QF4A512 External Clock connection

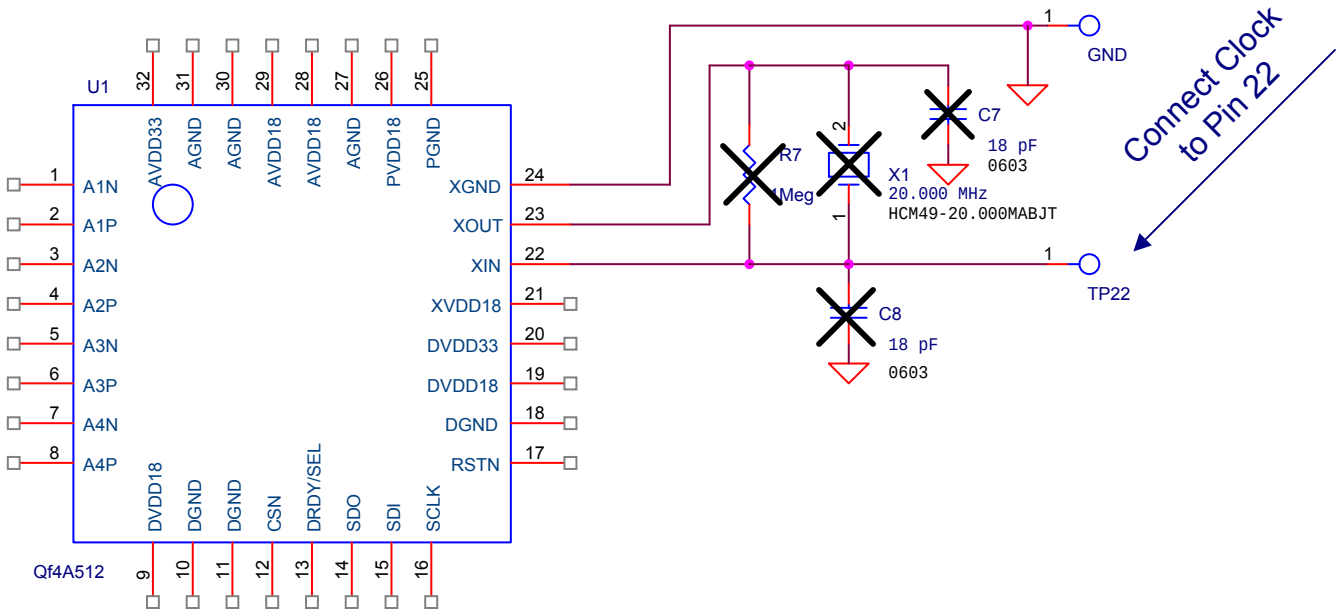


Figure 2:

4)

5) Software The Clock input is defaulted to the 20 MHz crystal required by the evaluation board. See figure 3.

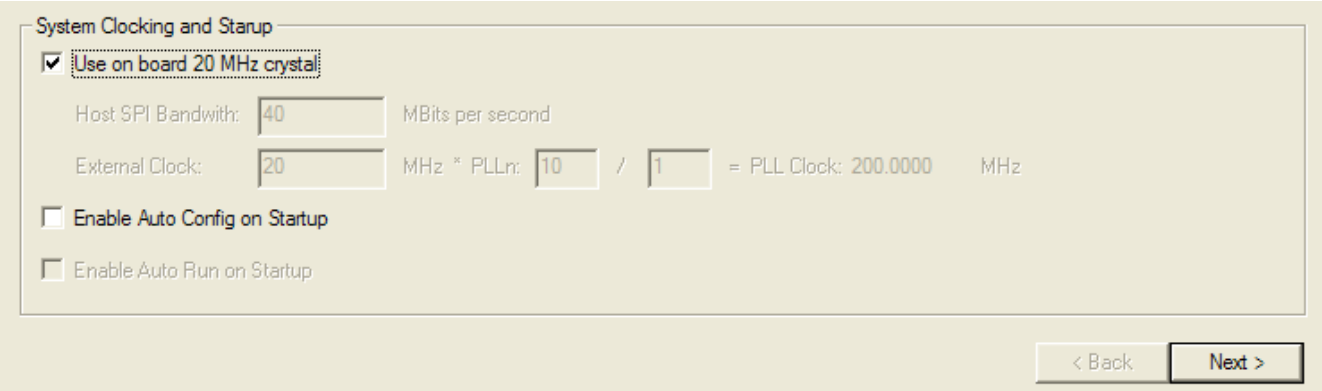


Figure 3:

If you wish to use a source other than the 20 MHz crystal on the evaluation board Uncheck the "Use 20 MHz crystal on development board". See Figure 4.

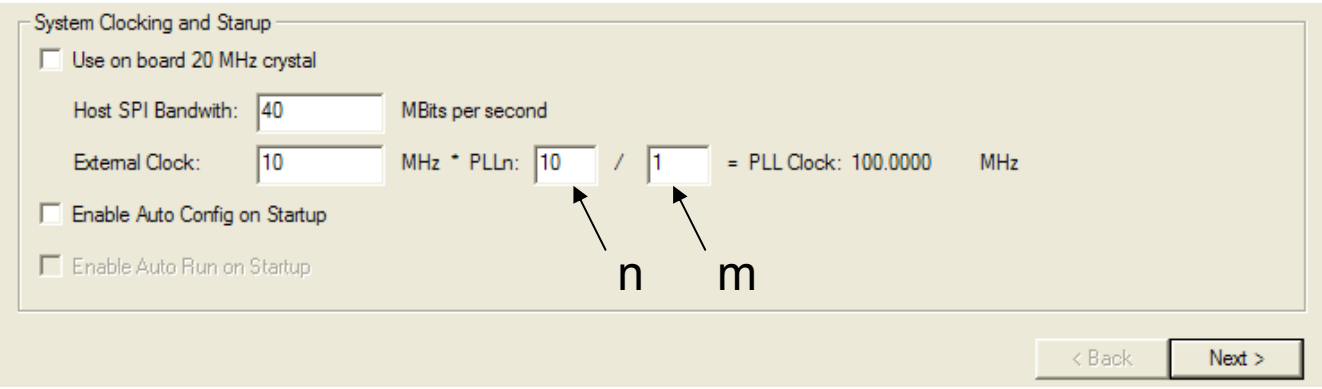
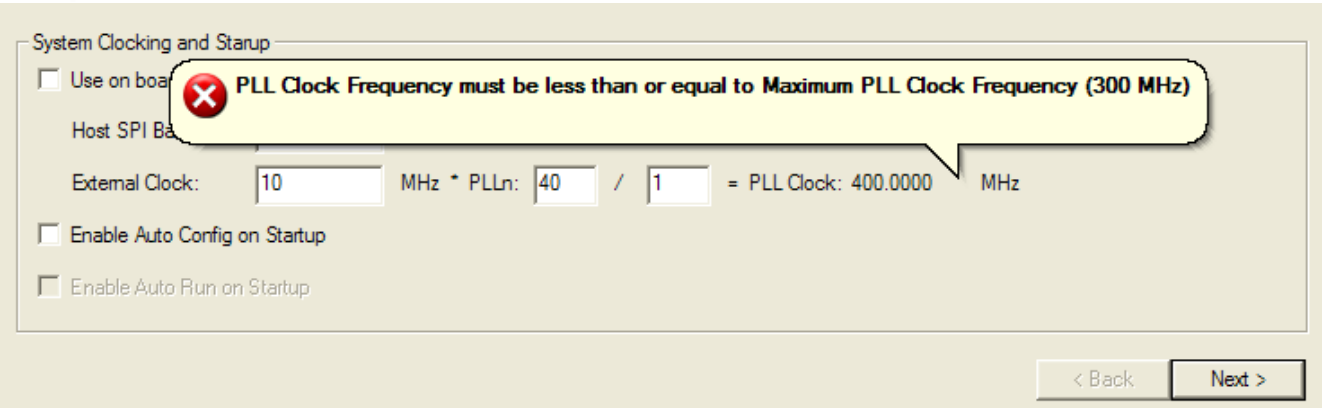


Figure 4:

In this example, the designer typed in a 10 MHz crystal, or external clock source in the External Clock field, 10 for the PLLn value, and 1 for the PLLm value. The result equaled a PLL clock of 100 MHz. Quickfilter software computes the rest of the required internal clock calculations for the designer. Although many combinations are legal, generally a lower PLL clock will use less power than the standard 200 MHz. The Quickfilter software takes the designer chosen PLL clock and makes the internal ADC clock as well as the system clock as low as possible. If one of the parameters is out of range, a warning message comes up when the "NEXT" button is selected. See Figure 5.



Designer's note – The following equations are the rules which Quickfilter software calculates the appropriate minimum internal clocks. The equations are for the designers information only when deciding on n and m. Generally m can be left at "1" Range (63 to 1) and n can be adjusted Range (63 to 1).

Debug note – Although the minimum range is 5 MHz, the actual filter design may call for higher input frequency see equation below.

Theory:

Rule #1 The PLL clock has to range from 20 to 300 MHz.
Rule #2 The PLL clock = Input Clock Freq * (n/m)
Rule #3 The Input External Clock must range from 5 to 300 MHz.
Rule #4 The internal ADC Clock ranges from 12.5 to 100 MHz. (This is based on the PLL clock/ 2,4,8 or 16)

Rule #5 The system clock = PLL clock/2^N where N= 1-6 where system clock must:

System clock ≥ ((Number of Taps +1)/2)+1)*sampling frequency
System clock ≥ 104 * sampling frequency
System clock ≥ 3 * SCLK/16 (for 1 channel high speed mode 16 bits out)
System clock ≥ 3 * SCLK/24x (where x=number of enabled outputs)

6) Summary

Input PLL m/n was adjusted from 10:1 to 4:1, also PLL_CTRL_0 bit 6 PLL range was changed from 1 to 0 making it the 20MHz to 100 MHz range.
This brought the actual band pass from 5KHz to 2KHz at 20MHz in our software.

Conclusion:

Cobra was capable of moving a fixed 100 tap band pass filter from 250 Hz to 6KHz by changing the input clock from 2.5MHz to 60MHz.
See the following range:

125 Hz = 1.25MHz (did not work)
250 Hz = 2.5 MHz (worked but out of specified range)
500 Hz = 5 MHz
1 KHz = 10 MHz
2 KHz = 20 MHz
4 KHz = 40 MHz
5 KHz = 50 MHz
6 KHz = 60 MHz (worked but out of chips specified range)
7 KHz = 70 MHz (did not work)

7) Summary

The QF4A512 Programmable Signal Converter can run from 5 MHz to 300 MHz from an external clock source by simply typing in the correct values for the internal phase lock loop PLL “n” and “m”.

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