Power Optimization for the QF4A512 Programmable Signal Converter

1) Introduction

This Application Note describes several methods by which power consumption can be substantially reduced.

Quickfilter software optimizes the internal clock settings automatically to minimize power consumption based on the currently loaded filter design. Lowering the ADC sample rate reduces power consumption since the system clock will be lowered accordingly to match the required sample rate.

Additionally, applications can save power by utilizing Power Off, Shutdown, and Sleep Modes. Average power consumption may be dramatically reduced by leaving the part in one of the power saving modes when data is not required then waking the part only long enough to take the necessary data.

This Application Note describes the following:

- Power saving modes.
- Power consumption details for both 1.8V and 3.3V supplies
- Power consumption vs. sampling rate vs. number of used taps.

2) Power Saving Modes

Cold Start: Disconnect all power to the QF4A512 during intermittent measurement times. Power required 0 mW. Startup time is less than 10ms. When power is re-applied, startup is automatic with auto-configure and auto-start activated. A MOSFET or switched LDO can be used for power disconnect. A majority of the startup time comes from loading the 4K bytes of data from EEPROM into the QF4A512's RAM and is determined by the EEPROM clock rate (eeclk_rate). The default eeclk_rate is 1.25 MHz set in register 07h hex. For the quickest startup time change this rate to 5 MHz. See Note1 on page 2.

Power Down: Shut down the oscillator, Phase Lock Loop (PLL) and Analog to Digital Converter (ADC) during intermittent readings. *Power required <1 mW.* Startup time is less than 1 ms.

Normal Power up: The QF4A512 uses nominal quiescent power typically 2 mW. The oscillator and PLL are running but the rest of the part is in Standby Mode. Start up time is immediate.

Power Saving Modes:

Mode	Quiescent Power	Startup Time
Cold start	0 mW	< 10ms
Power Down	<1 mW	< 500µs
Normal	<3 mW	Immediate

Table 1

*Note 1

The eeclk_rate can be programmed by writing directly to register 07h in the QF4A512. If using the typical XTAL frequency of 20 MHz, you would select 20 frequency/4 = 5 MHz which is done by entering “010” in bits 6, 5, and 4 respectively. See the register information below taken from the data sheet.

07h STARTUP (SPI Setup)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 07h	X	eeclk_rate2	eeclk_rate1	eeclk_rate0	0	0	auto_start	auto_config

Bit 0

auto_config

* 0 = Does nothing.

1 = Data copied from EEPROM

Description: Automatically loads chip configuration registers and FIR coefficients into RAM.

Bit 1

auto_start

* 0 = Configure mode.

1 = Run mode

Description: In Run mode automatically starts filtering and sending out filtered data on the SIF interface.

Bits 3,2

Always 0

Bits 6,5,4

eeclk_rate

000 (110, 111) = XTAL frequency

001 = XTAL frequency/2

010 = XTAL frequency/4

011 = XTAL frequency/8

*100 = XTAL frequency/16

101 = XTAL frequency/32

Description: Clock Rate for EEPROM data transfer. Frequency is divided down as shown above. Maximum value is 5, higher values if written will default back to 000.

Bit 7

Don’t care

3) Power consumption details.

The QF4A512 Programmable Signal converter uses both a 3.3V supply and a 1.8V supply. The following is a block diagram showing by color which sections of the chip are powered by 1.8V Digital, 1.8 Analog, 3.3V Digital, and 3.3V Analog.

Blue= 3.3V Analog, Orange= 1.8V Analog, Red= 1.8V Digital, Green= 3.3V Digital.

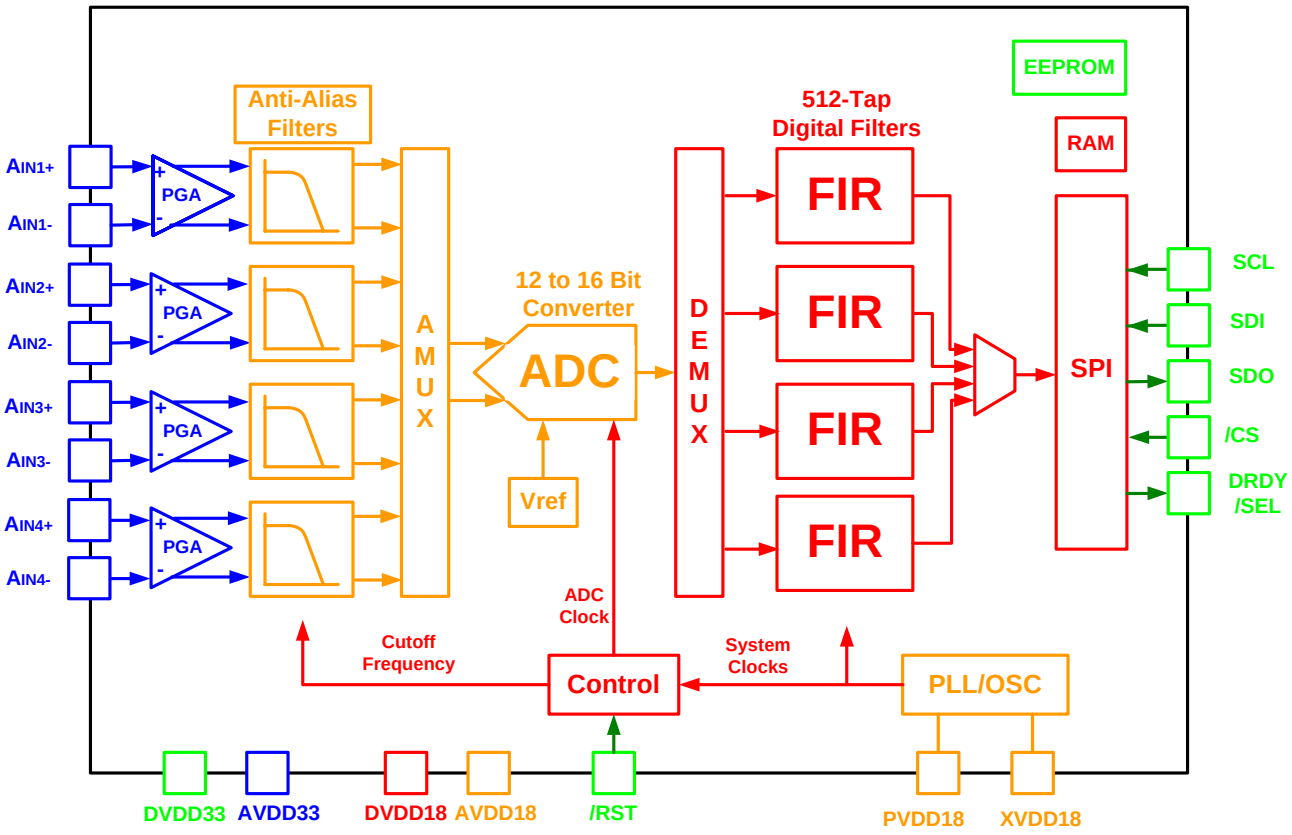

Figure 1

Designers Note:

Average Power is the typical power draw taken from experimental data. The maximum power is the theoretical limit given for power supply design constraints.

Graphs showing supply current for 1 kHz, 100 kHz, and 2.5 MHz.

	3.3V Digital AVG (mA)	MAX	3.3V Analog AVG (mA)	MAX	1.8V Digital AVG (mA)	MAX	1.8V Analog TYP (mA)	MAX	Power AVG (mW)	MAX
Quiescent Power	0.15	mA	0.01	mA	0.29	mA	0.53	mA	**2.00**	**mW**
Typical Power Down	0.10	mA	0.01	mA	0.28	mA	0.05	mA	**0.96**	**mW**
Sample Rate 1 kHz	**AVG**	**MAX**	**AVG**	**MAX**	**AVG**	**MAX**	**TYP**	**MAX**	**AVG**	**MAX**
Typical 1Ch	0.09	0.20	4.36	5.00	3.42	4.00	35.54	36.00	**84.82**	90.00
Typical 2Ch	0.08	0.20	8.59	9.00	5.58	6.00	55.28	56.00	**138.16**	142.00
Typical 3Ch	0.06	0.20	12.74	13.00	6.82	8.00	72.80	74.00	**185.57**	192.00
Typical 4Ch	0.05	0.20	16.82	17.00	8.04	9.00	89.03	90.00	**230.38**	235.00
Sample Rate 100 kHz	**AVG**	**MAX**	**AVG**	**MAX**	**AVG**	**MAX**	**TYP**	**MAX**	**AVG**	**MAX**
Typical 1Ch	0.16	0.30	4.37	5.00	4.63	5.00	35.56	36.00	**87.30**	92.00
Typical 2Ch	0.17	0.30	8.60	9.00	10.39	11.00	60.48	62.00	**156.48**	163.00
Typical 3Ch	0.13	0.30	12.64	13.00	19.58	20.00	89.30	90.00	**238.13**	242.00
Typical 4Ch	0.13	0.30	16.66	19.00	23.93	25.00	104.97	106.00	**287.43**	300.00
Sample Rate 2.5 MHz	**AVG**	**MAX**	**AVG**	**MAX**	**AVG**	**MAX**	**TYP**	**MAX**	**AVG**	**MAX**
Typical 1Ch	0.09	0.20	4.24	5.00	71.87	73.00	75.50	76.00	**279.55**	286.00

Table 2

Power Pin assignment:

Pin	Pin Name	Type	Description
9	DV_{DD18}	Power	+1.8V DC Power (Digital)
10	DGND	Ground	Digital Ground
11	DGND	Ground	Digital Ground
18	DGND	Ground	Digital Ground
19	DV_{DD18}	Power	+1.8V DC Power (Digital)
20	DV_{DD33}	Power	+3.3V DC Power (Digital)
21	XV_{DD18}	Power	Filtered +1.8V DC Power for Internal Oscillator
24	XGND	Ground	Ground for Internal Oscillator
25	PGND	Ground	Ground for Phase Lock Loop
26	PV_{DD18}	Power	+1.8V DC Filtered Power for Phase Lock Loop
27	AGND	Ground	Analog Ground
28	AV_{DD18}	Power	+1.8V DC Power (Analog)
29	AV_{DD18}	Power	+1.8V DC Power (Analog)
30	AGND	Ground	Analog Ground
31	AGND	Ground	Analog Ground
32	AV_{DD33}	Power	+3.3V DC Power (Analog)

Table 3

Graph of Power Consumption vs. Channel Count vs. Sampling Rate.

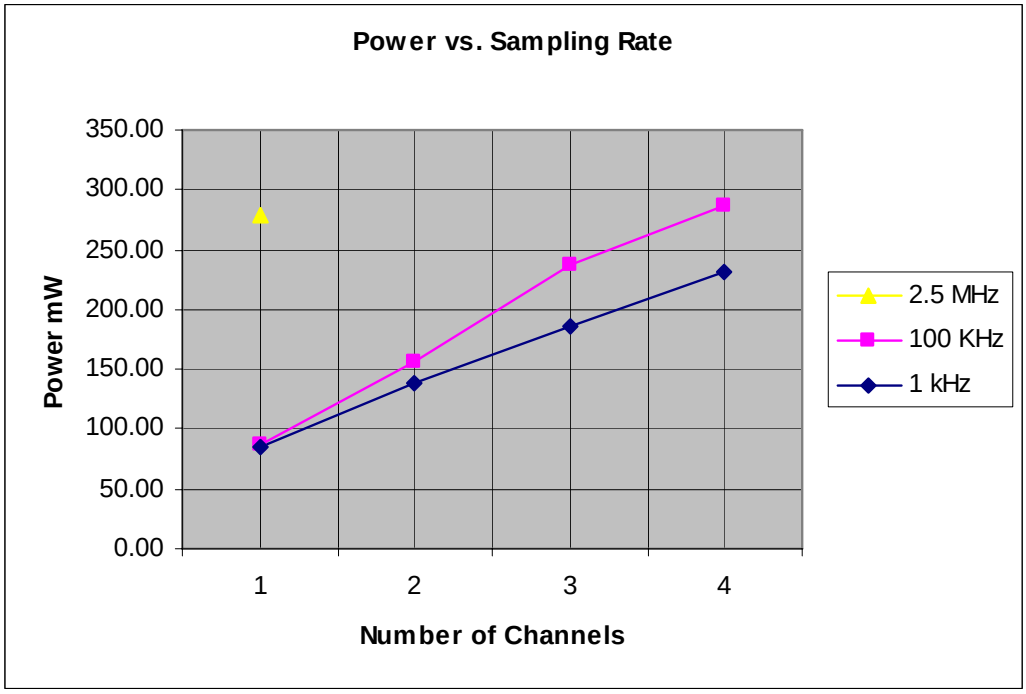

Figure 2

4) Power consumption vs. sample rate vs. number of taps.

Figure 2 shows sample rate vs. power vs. number of channels active. In general, the lower you can get the sample rate, the more power you will save.

There is no significant impact on total power consumption as a function of the number of taps used for a particular filter. However for the case of intermittent applications where the QF4A512 wakes up, takes data and then goes back to sleep, the number of taps adds to the latency of the signal passing through the QF4A512. The longer the latency (more taps), the longer it will take the part to move from operating mode to sleep mode thus increasing the average power consumption.

5) Summary

Quickfilter software automatically optimizes the internal clock settings for the best power savings. However, the designer can significantly reduce operating power consumption by adjusting the sample rate of the filter as low as possible which in turn will guarantee the system clock will be adjusted as low as possible. If the end application can intermittently measure data, various power saving methods can be applied to save power by waking up, measuring data and then going back to sleep.

1. Contact Information:

Quickfilter Technologies, Inc.
1024 S. Greenville Avenue, Suite 100
Allen, TX 75002-3324

General: info@quickfilter.net
Applications: apps@quickfilter.net
Sales: sales@quickfilter.net
Phone: 214-547-0460
Fax: 214-547-0481
Web: www.quickfiltertech.com