Multiple Chip Configuration
QF4A512 Programmable Signal Converter

1) Introduction

This Application Note shows how to connect multiple QF4A512 programmable signal converters to a microprocessor's SPI bus detailing how to calculate the minimum required serial clock (SCLK).

This application note describes the following:

- Hardware connection using data ready (DRDY).
- Hardware connection (no DRDY)
- Basic approach for SCLK calculation.
- Advanced approach for efficient SCLK calculation.

2) Hardware connection using data ready (DRDY) for fastest performance.

Connecting Multiple IC's to the SPI using DRDY

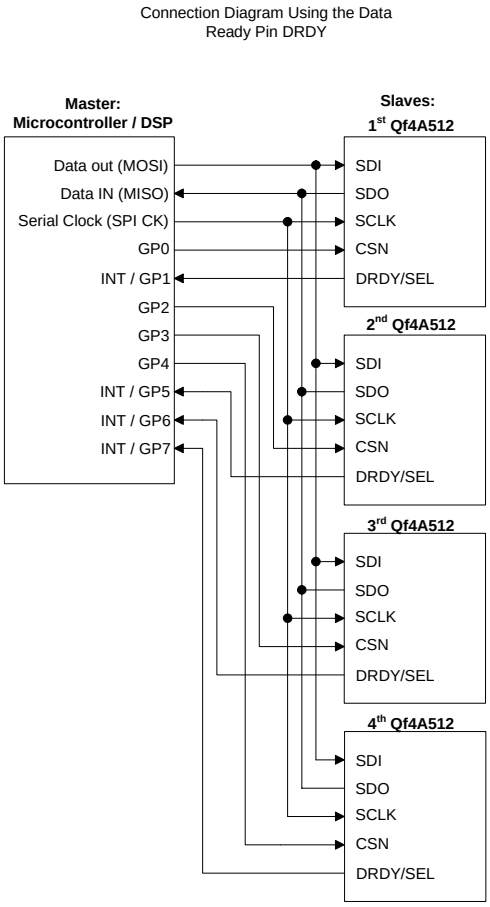

Figure 1

3) Hardware connection (no DRDY) signals used.

Connecting Multiple IC's on the SPI without Data Ready

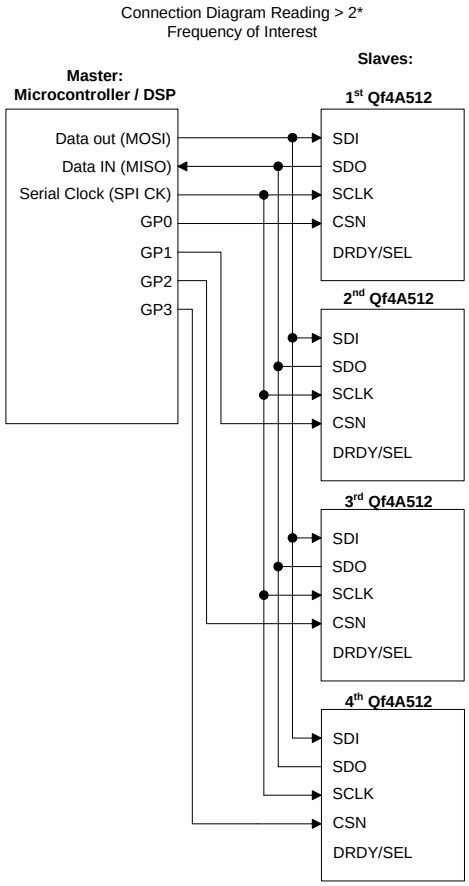

Figure 2

4) Basic approach for SCLK calculation using all channels at the speed of the fasted required sampled channel.

Calculating Required SCLK:

*Note: Quick Filter software will automatically determine the optimized minimum SCLK speed. This application note describes the minimum serial clock rate. If sampling at a higher rate simply replace (frequency range of interest) * 2.2 with the new faster sampling rate.*

Determine the highest incoming frequency of interest across all channels on all IC's if more than one. This approach spends an equal time between all IC's and channels receiving the data. The SPI clock rate can be calculated using the following formula for one or more IC's:

SR = Sampling Rate = (highest frequency range of interest) * 2.2

*Clock frequency (SCLK) >= SR * (# of monitored channels) * (Serial Word Length)*

This is the easiest approach using a single QF4A512, however it is less efficient if using multiple QF4A512's. The (# of monitored channels) in the above formula is equal to 4 per IC times the number of IC's used. If a channel is disabled subtract that channel from the total (# of monitored channels). Note the (Serial Word Length) would be 24 since multi-channel mode uses 24 bits.
Note: For a very high frequency measurement, you can reconfigure for single channel mode temporarily and get a faster rate out of the SPI see application note QFAN002. In this case, the above formula would reduce to: Clock frequency (SCLK) >= (highest frequency range of interest)*2.2*1*16.

Example 1:
Measuring 2 kHz as the highest frequency range on 16 channels (4 IC's) using multi-channel mode (24-bits)
Clock frequency = (2K) * 2.2 * (16) * (24) = 1.690 MHz, so an SCLK of 2.048 MHz would guarantee receiving the data faster than the desired frequency.

Example 2:
Measuring 1.1 MHz frequency range on 1 channel using single channel mode (16-bits)
Clock frequency = (1100K) * 2.2 * (1) * (16) = 38.72 MHz, so an SCLK of 40 MHz would guarantee receiving the data at the desired frequency.

Example 3:
Measuring 50 kHz frequency range on 3 channels using multi-channel mode (24-bits)
Clock frequency = (50K) * 2.2 * (3) * (24) = 7.920 MHz, so a common SCLK of 8.192 MHz would guarantee receiving the data faster than the desired frequency.

Example 4:
Measuring 40 kHz on 4 channels using multi-channel mode (24-bits)
Clock frequency = (38K) * 2.2 * (4) * (24) = 8.026 MHz, so a common SCLK of 8.192 MHz would guarantee receiving the data faster than the desired frequency.

5) Advanced approach for efficient SCLK calculation.

Polling the slower sampling rate QF4A512's in multiple IC system less frequently requires less serial clock SCLK bandwidth.

Calculating Required SCLK:
Determine the highest incoming frequency of interest for each QF4A512. The SCLK frequency needs to be at least the value of the highest frequency times 2.2 (minimum sample rate) times the number of enabled channels.

This needs to be calculated for each QF4A512 in the system. From here a minimum SCLK frequency can be found by polling each QF4A512 IC at a percentage of time to ensure updating the incoming information by the following formula: (Note $n^{th} = 5^{th}, 6^{th}, 7^{th}$ etc IC used in the system. SR = Sampling Rate = highest frequency of interest * 2.2)

*Clock frequency (SCLK) >= {[(First IC's highest SR)*number of channels used] + [(Second IC's highest SR)*number of channels used] + [(Third IC's highest SR)*number of channels used] + [(Fourth IC's highest SR)*number of channels used] +…+ [(n^{th} IC's highest SR)*number of channels used)]}* (Serial Word Length = 24 in Multi-Channel Mode)*

In order for this method to work, the designer needs to poll the particular IC at a percentage of the time based on the following formula:

*% of polling 1^{st} IC = [(1^{st} IC's highest SR)*number of channels used] / {[(1st IC's highest SR)*number of channels used] + [(2^{nd} IC's highest SR)*number of channels used] +…+ [(n^{th} IC's highest SR)*number of channels used]}*

This same formula can be used to determine the polling frequency for the 2nd QF4A512 IC by swapping 1st and 2nd etc...
This method will reduce the necessary SCLK rate significantly if one QF4A512 is measuring much lower frequencies than another QF4A512 IC.

Example 5:
Measuring 1 kHz on the first IC, 18 kHz on the second IC, 100 Hz on the third IC, and 5 KHz on three channels on the fourth IC using multi-channel mode (24-bits).
SCLK > [(1K*4 + 18K*4 + 100*4 + 5K*3) * 2.2 * 24] = 4.826 MHz, so a SCLK of 5 MHz would guarantee receiving the data faster than the frequencies of interest.
Note: The percentage of time necessary for polling the 1^{st} IC for new data would be: % of 1^{st} IC = (1K*4)/(1K*4 + 18K*4 + 100*4 +5K*3) = 5% of the time @ 4.096 MHz.

Debug Note

Be sure to allow at least a 5% margin increase from the calculated SCLK speed in order to accommodate microprocessor internal overhead for things such as CS between different QF4A512's etc.

6) Summary

The serial clock speed requirement used for the SPI system interface can be greatly reduced for multi chip systems by using intelligent polling schemes between IC's. The use of the data ready pin through interrupts maximizes system efficiency.

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