APPLICATION NOTE **QFAN004**

Interfacing Analog Signals to the QF4A512 Programmable Signal Converter

1) Introduction

This Application Note describes how to connect an analog signal to Quickfilter's QF4A512 Programmable Signal Converter. Applications can be connected in single ended or differential mode, as well AC or DC coupled.

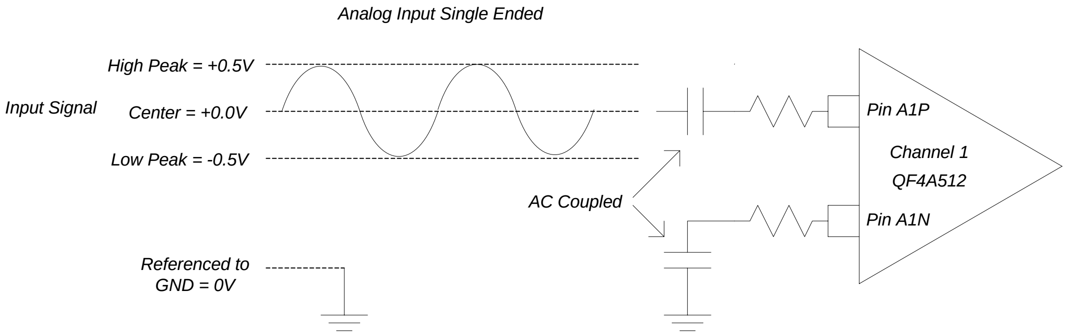
This application note describes the following:

- AC and DC coupling.
- Determining correct gain setting resistors.
- Understanding the Digital output relative to the Analog input signal.
- Choosing the correct coupling capacitors.

2) What type of analog signal do you need to measure?

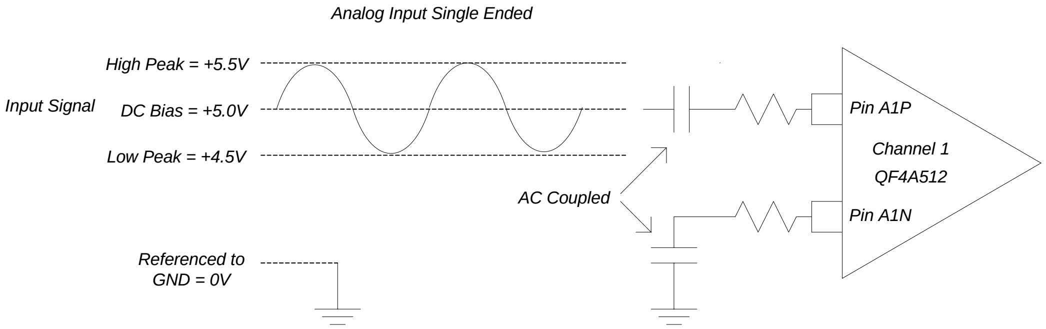
Choose from one of the 4 following examples for your application.

Example 1: The signal is an AC signal referenced to ground (Single Ended).
Solution: AC couple to remove any DC bias effects.



Or:

The signal is an AC signal riding on a DC Bias (Single Ended).
Solution: AC couple to remove any DC bias effects.



Theory:

In this example the coupling capacitor isolates both the external +5V DC bias from railing the input signal as well as correctly referencing the internal +1.16V DC bias. See section 4 (Choosing a coupling capacitor).

The linear range of the input Pin is between +0.5V and +2.5V. Since we properly set up the signal swing for +/- 0.5V (0-1Vpp), the range will be +0.7V to +1.7V. The full scale range digitally is +/- 1V. However, if we scaled the input voltage to be +/- 1V we would get 0.2V to 2.2V which violates the minimum +0.5V rule.

Therefore for the correct +/- 0.5V input swing, we have half of the digital range. To correct this, simply multiply the PGA gain x2.

Formula: (Only applicable for voltages => 1Vpp) For lower voltages use higher PGA gain and no series resistors.
Input Series Resistors R1-R8 = (Input Voltage * 10K) – 10K

Here is a table of desired input voltages and what the added series resistor should be including the correct PGA setting for full scale digital output.

Solutions for Example 1:
(Gives 2Vpp into the ADC for full digital output range)

Desired AC Input Voltage	Input series resistors R1-R8	PGA setting
0 to +0.25Vpp	**0 Ohms**	**x8**
0 to +0.5Vpp	**0 Ohms**	**x4**
0 to 1Vpp	**0 Ohms**	**x2**
0 to 2Vpp	**10K**	**x2**
0 to 3Vpp	**20K**	**x2**
0 to 3.3Vpp	**23K**	**x2**
0 to 5Vpp	**40K**	**x2**
0 to 10Vpp	**90K**	**x2**
0 to 12Vpp	**110K**	**x2**
0 to 15Vpp	**140K**	**x2**
0 to 20Vpp	**190K**	**x2**
0 to 24Vpp	**230K**	**x2**
0 to 28Vpp	**270K**	**x2**

Table 1

Example Schematic for AC coupled Single Ended applications:

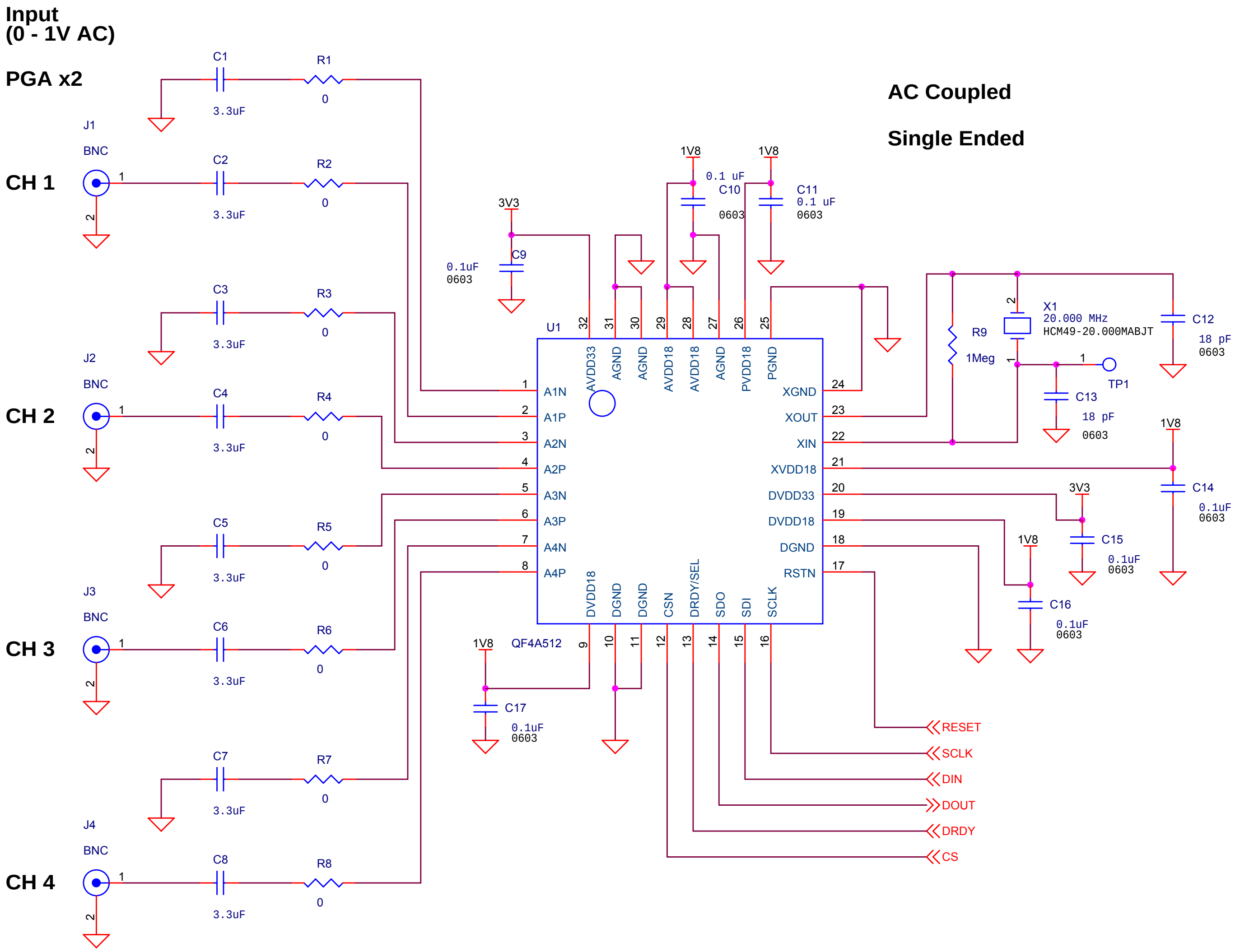
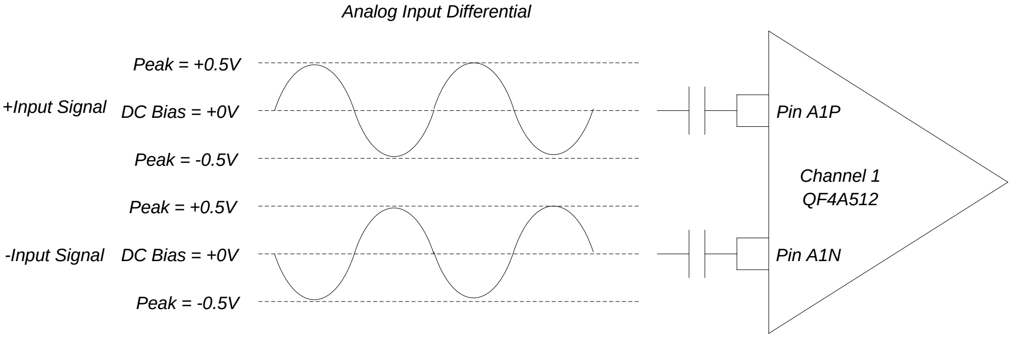


Figure 1

Example 2: The signal is a Differential AC signal.
Solution: AC couple to remove any DC bias effects.



Theory:
In this example the coupling capacitors correctly isolate the internal +1.2V DC bias on both inputs. See section 4 (Choosing a coupling capacitor).

Each input to the QF4A512 needs to stay between +0.5V and +2.5V. Since we properly set up the signal swing for +/- 0.5V on each input, the range will be (+0.7V to +1.7V) times two since it's differential. The full scale range digitally is 2Vpp. Although each input signal is only 1Vpp in amplitude, the resulting differential signal is 2Vpp. Therefore we can achieve the full digital output range with the PGA set to x1.
See Section 3 (Understanding the digital output relative to the analog input signal)

Formula: (Only applicable for voltages => 2Vpp) For lower voltages use higher PGA gain and no series resistors.
Input Series Resistors R1-R8 = ((Input Voltage/2) * 10K) – 10K

Solutions for Example 2:
(Gives 2Vpp into the ADC for full digital output range)

Desired AC Input Voltage	Input series resistors R1-R8	PGA setting
0 to +0.25Vpp	0 Ohms	x8
0 to +0.5Vpp	0 Ohms	x4
0 to 1Vpp	0 Ohms	x2
0 to 2Vpp	0 Ohms	x1
0 to 3Vpp	5K	x1
0 to 3.3Vpp	6.5K	x1
0 to 5Vpp	15K	x1
0 to 10Vpp	40K	x1
0 to 12Vpp	50K	x1
0 to 15Vpp	65K	x1
0 to 20Vpp	90K	x1
0 to 24Vpp	110K	x1
0 to 28Vpp	130K	x1

Table 2

Example Schematic for AC coupled Differential applications:

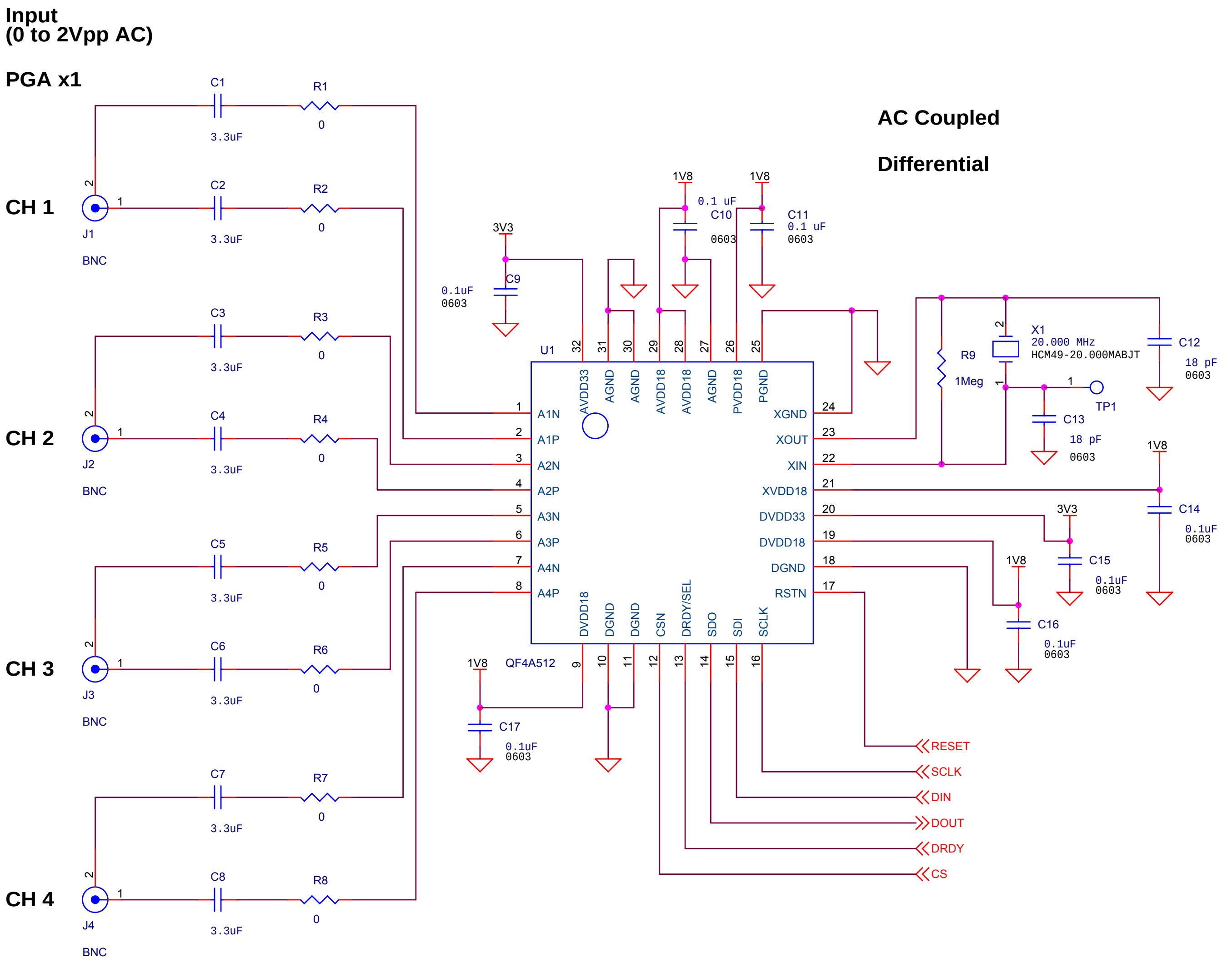
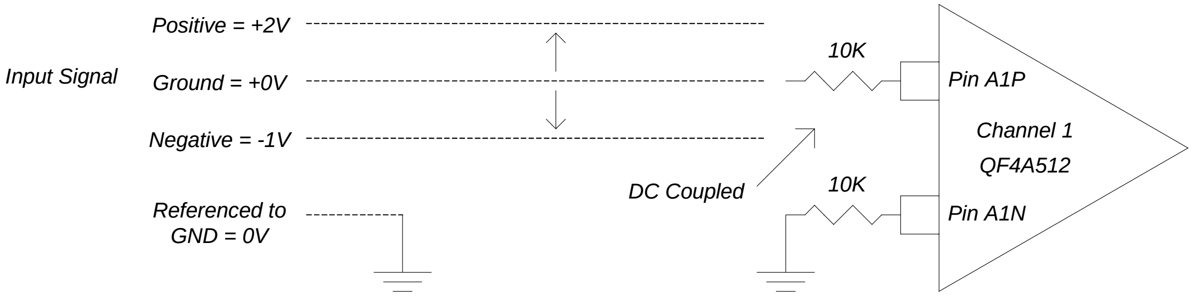


Figure 2

Example 3: The signal has a DC component referenced to ground that needs to be measured, and, or very low AC frequencies which would require too large of a capacitor to couple.
Solution: DC couple (DC Single Ended).

Analog Input DC Single Ended



Theory:
The QF4A512 inputs can measure negative voltages. There are two important points to understand. For AC signals we recommend staying between +0.5V and +2.5V on the input pins. For DC signals you can bend the rule and measure signals from +0.2V to +2.5V on the input pins. So how do you measure negative voltages when the input pins need to stay positive? That's an easy answer. You need matched resistors of at least 10K going to ground and in series with your signal to be measured. The negative voltage at the input (A1P) is divided by the resistor network to result in a voltage at the device pin (A1P) within the allowed range. However this voltage is less than the voltage at the A1N pin resulting in a negative differential input to the chip. This gives the digital output in 2's compliment a negative reading. If you look at the table below, you will see that when higher matched series resistors are used you can measure the full swing both plus and minus for a given range. That's because the input series resistor is high enough to not cause the input pin to go below +0.2V even though the input signal is say -12V.

The second point to note is that the internal reference voltage of +1.16V which you can measure floating at the input node of either the plus or minus inputs is protected from the other channels through an internal network. The good news is that one channels reference voltage is not affected by what is happening on the other channels. The bad news is that in the case of direct coupling, that particular channels reference voltage will drop by as much as 15% when loaded to ground with a 10K resistor. This will give a slight gain error for the signal you are measuring. This can be adjusted in software by adding 10% to a DC voltage reading when using lower series resistance like 10K. For the larger series resistors like 270K there is only a 5% drop. Recall that the QF4A512 has an internal resistor of 10K. (Note this internal resistor may vary from 8K to 12K) System calibration is required for making an accurate DC measurement. (See calibration application note QFAN012) The two external input series resistors need to be matched as closely as possible to avoid DC offset, preferably 1% or better tolerance, although this can also be corrected by performing a system calibration.

Solutions for Example 3:
(Positive range gives half of the 2’s compliment digital output range 0000h to 7FFFh)
(Negative range gives half of the 2’s compliment digital output range C000h to FFFFh)

Desired DC Input Voltage	Series resistors R1-R8	PGA setting
-0.1V +0.25V	10K	x8
-0.25V to +0.5V	10K	x4
-0.5V to 1V	10K	x2
-1V to 2V	10K	x1
-1.5V to 3V	20K	x1
-2V to 3.3V	23K	x1
-5V to 5V	40K	x1
-10V to 10V	90K	x1
-12V to 12V	110K	x1
-12V to 12V	230K	x2
-15V to 15V	140K	x1
-20V to 20V	190K	x1
-24V to 24V	230K	x1
-28V to 28V	270K	x1

Table 3

Here is an example of a single ended 3.3V DC input with the external resistors and the QF4A512 internal circuitry.

(Note the actual 1.16V internal reference is shown as 1.2V for simplicity)

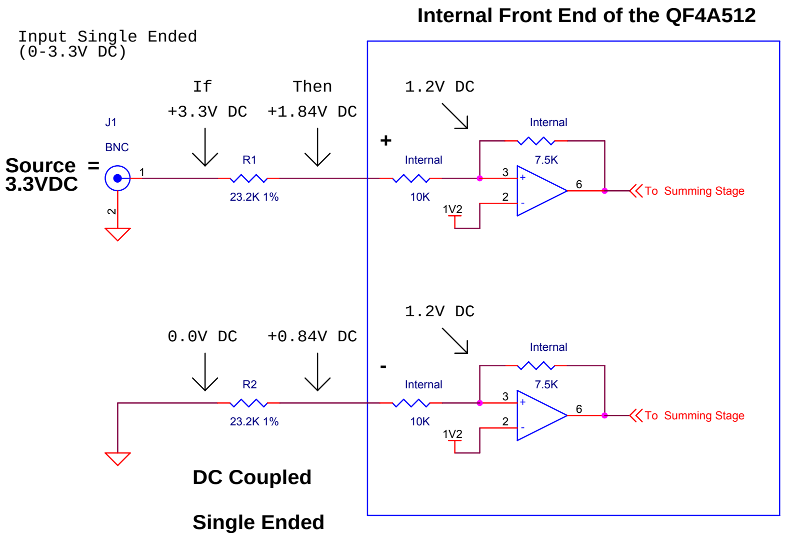


Figure 3

Here are the equations to show what's actually happening in the 3.3V case.

Case of Source = +3.3V to 0V DC

Positive input = [(3.3V – 1.2V) * (10K/(23.2K+10K))] + 1.2V = 1.84V
Negative grounded input = 1.2V * (23.2K / (23.3K+10K) = 0.84V

Looking at the positive to negative input with +3.3VDC gives:

1.84VDC – 0.84VDC = 1.0VDC x1 (PGA) = 7FFFh (digital output in hex)

Looking at the positive to negative input with 0VDC gives:
0.84V – 0.84V = 0V x 1(PGA) = 0000h (digital output in hex)

Negative voltages work the same way however the output shows negative in 2's complement.

Quickfilter software shows both negative and positive DC voltages in the "View DC" screen

Example Schematic for DC coupled Single Ended applications:

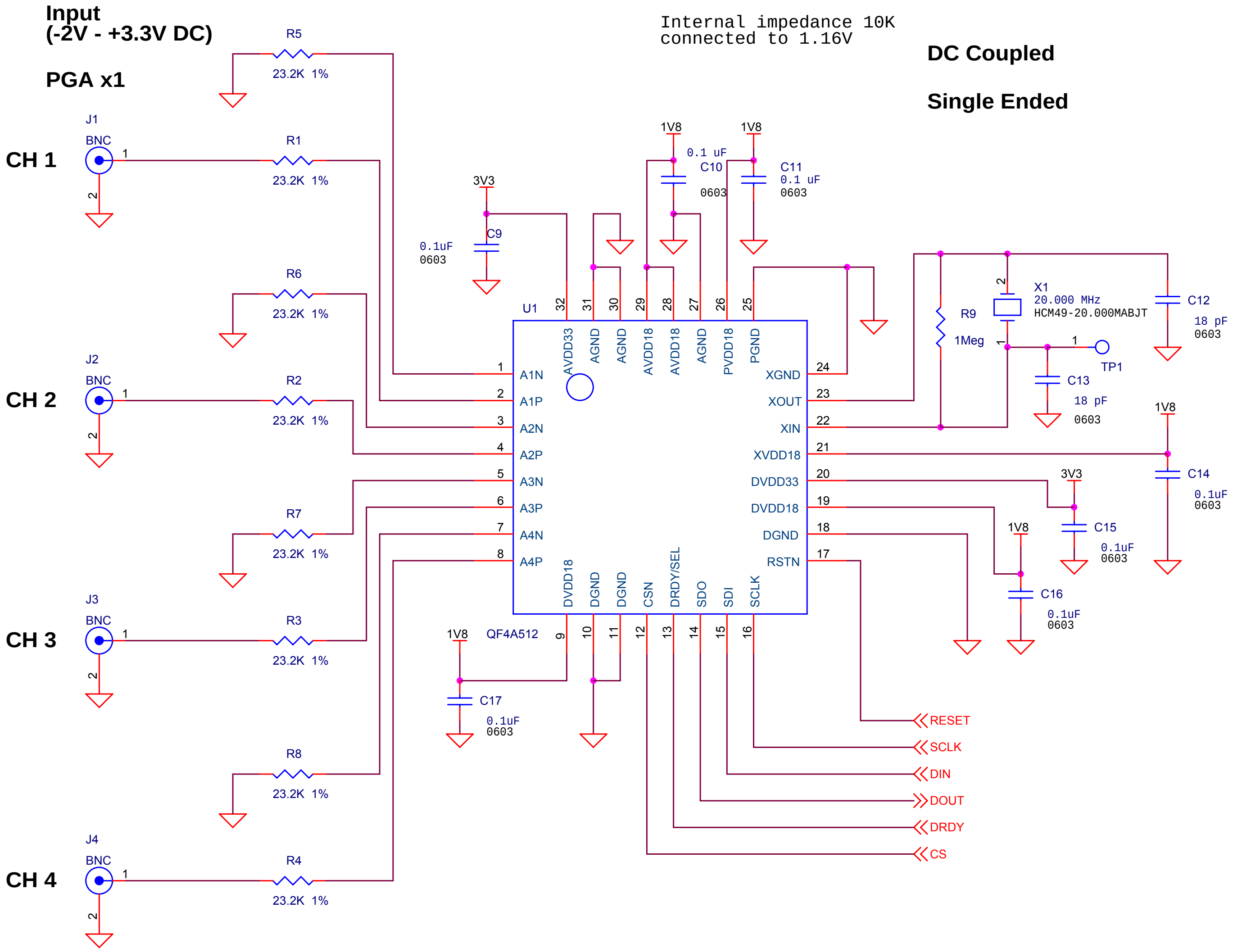
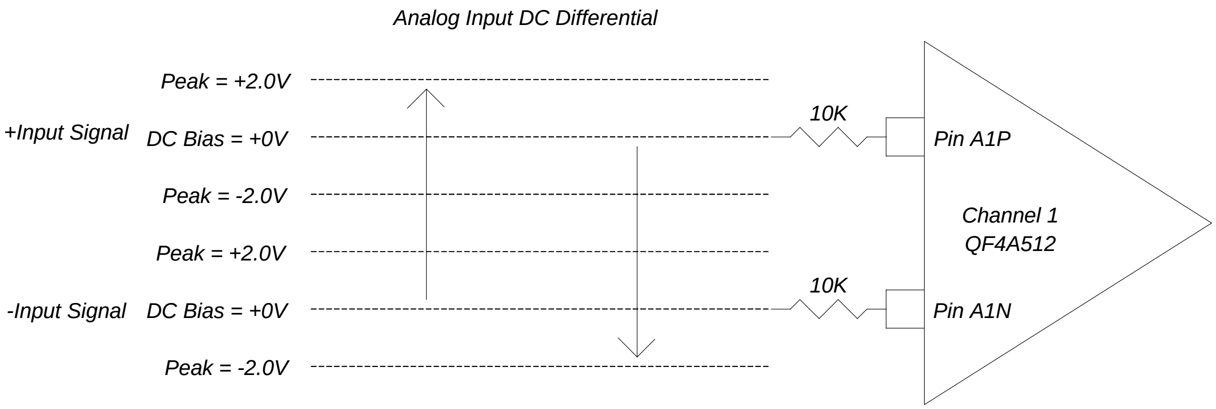


Figure 4

Example 4: The signal has a DC differential component that needs to be measured, and, or very low AC frequencies which would require too large of a capacitor to couple. Solution: DC couple (DC Differential). In the below example, a 2V maximum differential is allowed. Zero to +2V, or Zero to -2V, or -1V to +1V etc.



Theory:
The QF4A512 inputs need to stay between +0.2V and +2.5V with respect to DC. This can be easily accomplished by maintaining a minimum series resistance of 10K externally to each DC source. The resistors need to be matched as closely as possible to avoid DC offset, preferably 1% or better tolerance.

(See Theory of DC single ended example 3)

Solutions for Example 4:
(Positive range gives half of the 2's compliment digital output range 0000h to 7FFFh)
(Negative range gives half of the 2's compliment digital output range 8000h to FFFFh)

Desired DC Input Voltage	Series resistors R1-R8	PGA setting
-0.25V +0.25V	10K	x8
-0.5 to +0.5V	10K	x4
-1V to 1V	10K	x2
-2V to 2V	10K	x1
-3V to 3V	20K	x1
-3.3V to 3.3V	23K	x1
-5V to 5V	40K	x1
-10V to 10V	90K	x1
-12V to 12V	110K	x1
-15V to 15V	140K	x1
-20V to 20V	190K	x1
-24V to 24V	230K	x1
-28V to 28V	270K	x1

Table 4

Example Schematic for DC coupled Differential applications:

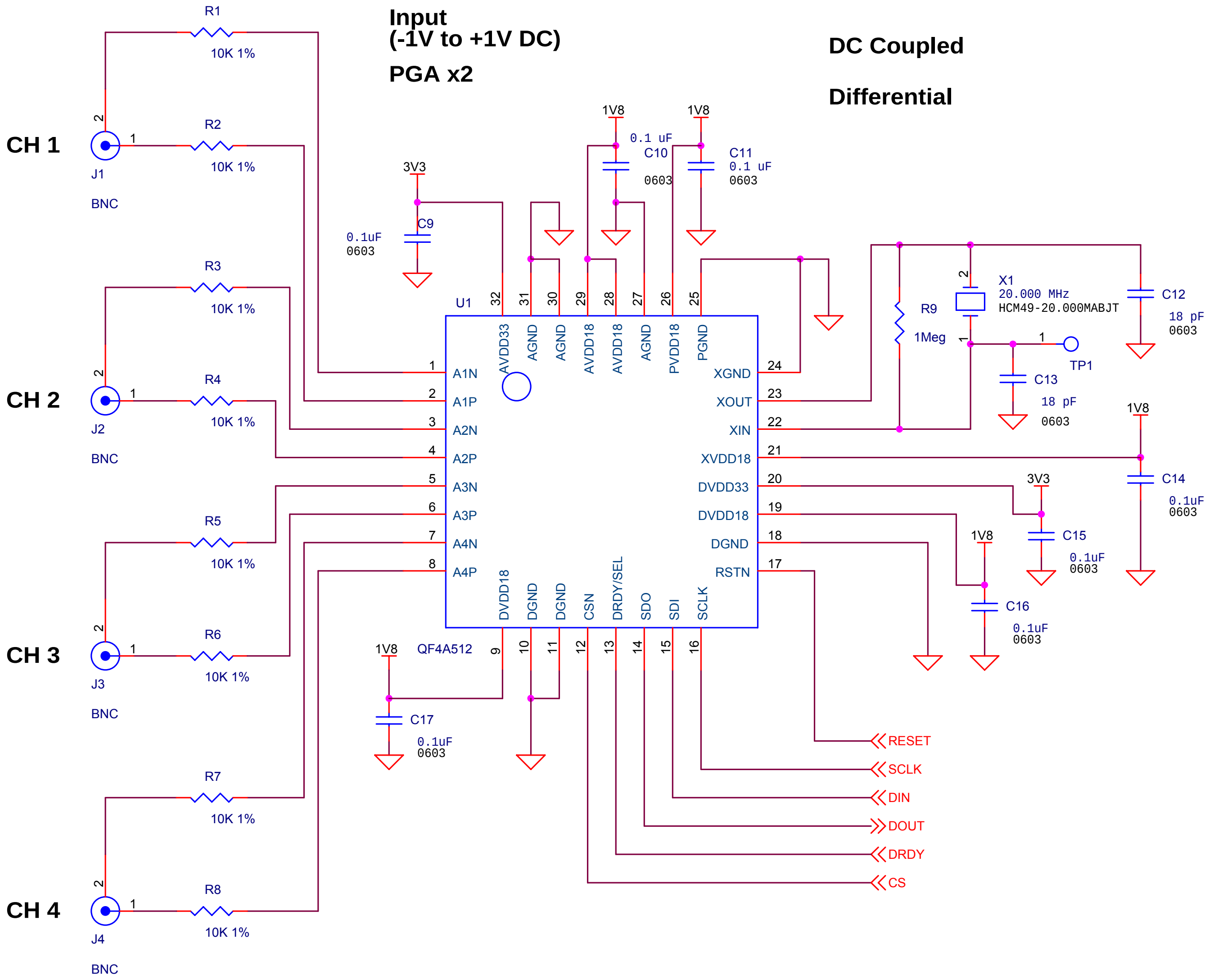


Figure 5

3) Understanding the Digital Output vs. the Input Analog Signal

Ideally the maximum input voltage to the QF4A512 should correspond to a full-scale reading from the ADC. If the input signal is too low to achieve this, then the PGA gain can be adjusted to provide a larger signal to the ADC. If the input signal is too high, then it should be attenuated with external series resistors to prevent clipping. Positive full-scale output from the ADC (7FFFh) will occur when the positive, A_{IN+}, is 1V more positive than the negative input, A_{IN-}. Negative full scale output (8000h) will occur when A_{IN+} is 1V more negative than A_{IN-}.

2's Complement refresher:
There are no negatives in Boolean algebra. This is why the 2's complement number system was devised. Two's complement is a way that lets us represent the entire numeric range in binary. This is done by taking the first significant bit and converting it for use similar to a +/- sign. A "1" proceeding a number means that number is negative, while a "0" means it is positive. Here are some examples:

Decimal		Binary
3	=	011
2	=	010
1	=	001
0	=	000
-1	=	111
-2	=	110
-3	=	101
-4	=	100

There is a simple process that converts normal binary to two's complement, and vice versa. Simply take your number, lets say 101, invert every number and add 1, like this:

```
  0101  (Number in unsigned binary)

  1010  (Bits inverted)
+ 0001  (Add a 1)
  -----
  1011  Your finished two's complement number.
```

The digital output from the QF4A512's Analog to Digital Converter is in "2's complement".

Output vs. Analog Input Table:

Voltage into ADC	PGA gain setting	Digital Output Hex 16 Bits	Digital Output Binary 16 Bits
+1.0V	x1	7FFFh	0111111111111111
+0.5V	x1	3FFFh	0011111111111111
0.0V	x1	0000h	0000000000000000
-0.5V	x1	C000h	1100000000000000
-1.0V	x1	8000h	1000000000000000

4) Choosing a coupling capacitor

Non-polarized:
Since a DC bias of 1.2V is present from the QF4A512, an incoming AC signal will cause a positive and negative voltage swing on the capacitor. For this reason it is recommended to use non-polarized capacitors, or two polarized capacitors back to back. Note: this halves the capacitance.

Voltage rating:
Make sure the voltage rating is at least 20% greater than the peak input voltage.

Types:
Ceramic capacitors are a good choice since they are by nature non-polarized and inexpensive however make sure they are low voltage to avoid non-linearities. For larger capacitive values required to pass lower frequencies electrolytic capacitors are a good choice as long as they are non-polarized. If polarized two of them can be put in series with the negative terminals connected forming a non-polarized capacitor. For ultra low noise instrumentation applications Polypropylene Film capacitors may be appropriate.

Capacitance:
The value of capacitor is determined by the lowest frequency of interest. A capacitor adds more series resistance (impedance) as the frequency is lowered. Since the QF4A512 has an internal resistance of 10K, there is a resistive series divide. If an external series resistor is added for gain adjustment this is also added to the series divide.

Formula for loss in the capacitor:

$1/(2\pi f)*C$. Where f is the frequency of interest, C is the capacitance value.

Example 1:
The resistance for a 1uF capacitor at 100 Hz would be 1/(2*3.14*100*0.000001) = 1592 Ohms. In this case with no additional input resistance the attenuation through the capacitor at 100Hz would be 1- (10K/(10K+1592)) = 13.7%

Example 2:
The resistance for a 0.1uF capacitor at 1 Hz would be 1/(2*3.14*1*0.0000001) = 1592000 Ohms. In this case with no additional input resistance the attenuation through the capacitor at 1 Hz would be 1- (10K/(10K+1.592M)) = 99.3%
For this low frequency, either a very large capacitor would have to be used, or best to use DC coupling.

5) Summary

Choosing from the appropriate AC or DC coupling examples above, quickly leads to the Correct Solution Table. The tables for each example give the correct external attenuation resistors and proper programmable gain setting for the desired analog input voltage. Using these values assures that the signal coming into the QF4A512 programmable signal converter gives full digital output in 2’s complement. If the desired input analog voltage was not shown, a formula is giving to calculate the correct attenuation resistors.

Contact Information:

Quickfilter Technologies, Inc.
1024 S. Greenville Avenue, Suite 100
Allen, TX 75002-3324

General: info@quickfilter.net
Applications: apps@quickfilter.net
Sales: sales@quickfilter.net
Phone: 214-547-0460
Fax: 214-547-0481
Web: www.quickfiltertech.com

The contents of this document are provided in connection with Quickfilter Technologies, Inc. products. Quickfilter makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in Quickfilter's Standard Terms and Conditions of Sale, Quickfilter assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.
Quickfilter's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of Quickfilter's product could create a situation where personal injury, death, or severe property or environmental damage may occur. Quickfilter reserves the right to discontinue or make changes to its products at any time without notice.

© 2005 Quickfilter Technologies, Inc.
All rights reserved.

Quickfilter, the Quickfilter logo and combinations thereof, are trademarks of Quickfilter Technologies, Inc.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.