Interfacing the ADS1251 to the QF1D512-DK Development Kit

1) Introduction

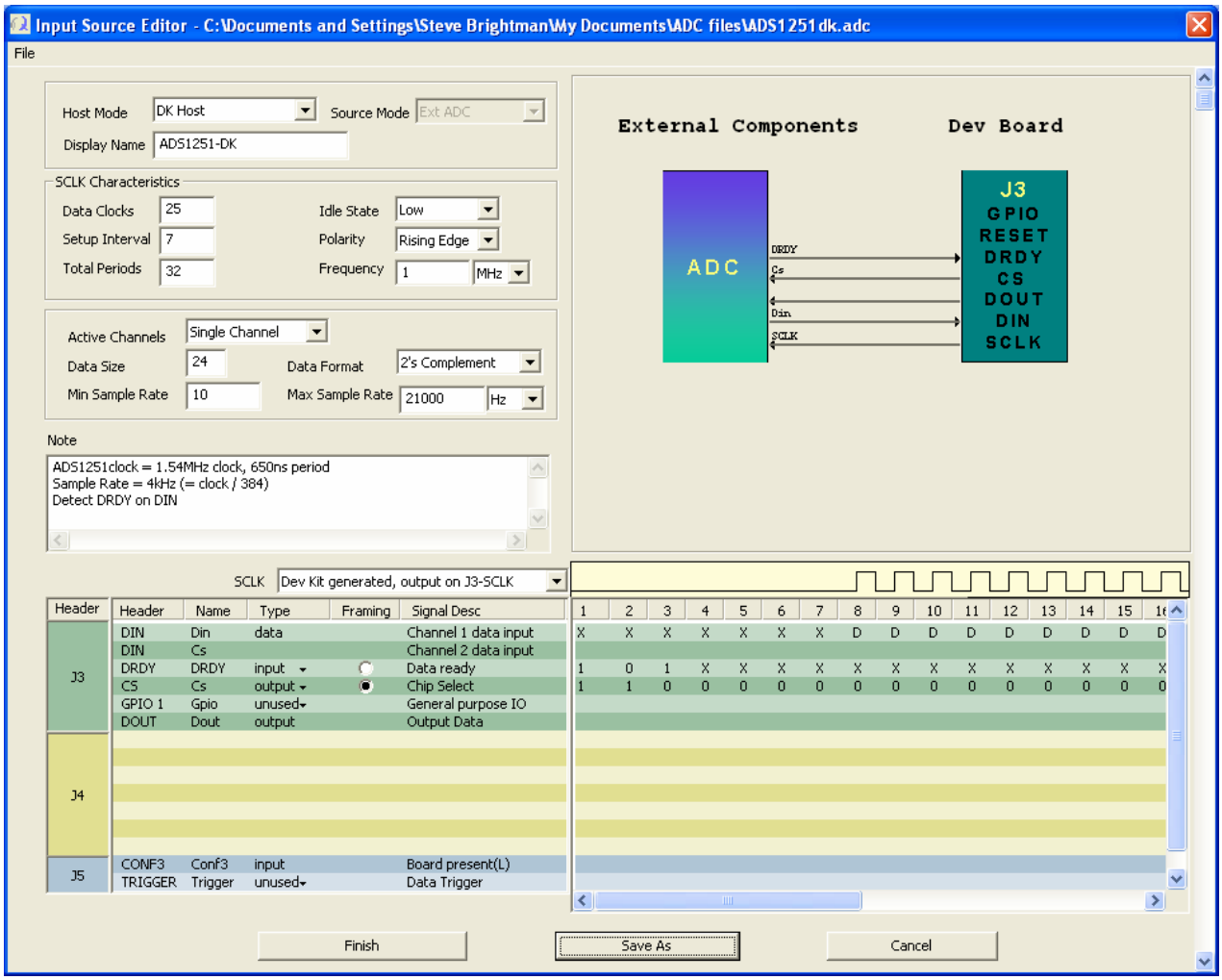
The ADS1251 is a 24-bit, 20kHz, Low-Power delta-sigma ADC from Texas Instruments. For evaluation purposes TI also offers a demo board, ADS1251EVM (see Section 4).

The ADS1251 requires an external master clock to be provided at up to 8MHz. The output data stream simply consists of 24 data bits but is slightly unconventional in that the output data pin also functions as the data ready output. No external chip select control signal is required. The user must detect the data ready signal and then provide 25 SCLK cycles to read out the conversion result.

2) Data Input Source File

The supplied file (**ADS1251dk.adc**) accomplishes the necessary task of detecting when new data is available and generating a framing signal to drive the DSEL pin of the QF1D512(s) on the development kit.

The start of a new output cycle is indicated by the output going high for 24 clock periods (t_4), then low for 6 clock periods (t_2), then high again for 6 clock periods (t_3). Subsequent rising edges on SCLK will then clock out the data, msb first. The ADS1251 data sheet also indicates a 25th cycle of SCLK after the lsb to complete the cycle (ADS1251 data sheet, figure 12).



In the Input Source Editor the DRDY signal is detected by the “101” sequence on the DRDY line. The FPGA will wait for the indicated transitions, however after DRDY goes high the second time we must delay the first edge on SCLK until after the 6 clock period duration of the DRDY signal (t_3). This is accomplished by adding additional setup intervals depending on the clock rate of the ADS1251 and the chosen SCLK rate. In the example shown, the ADS1251 clock rate has been set to 1.54MHz. Therefore time interval t_3 equals 3.9us (6 x 1/1.54). Our SCLK period is 1us (1MHz) so we need to allow 4 additional SCLK periods (periods 4 through 7 in the screenshot) after DRDY goes high the second time before the first SCLK to clock data from the device appears. The first SCLK appears in timeslot 8, signaling the start of the 24 bit data from the ADS1251.

A chip select signal is also generated. In the first setup interval CS is high, then is changed low for the remainder of the sample period. This signal is not required by the ADS1251 but provides the necessary framing signal for DSEL on the QF1D512.

Allowing for the 3 clock periods to detect 101 on DRDY and the 4 additional periods while DRDY remains high the “Setup Interval” has been set to 7 under “SCLK characteristics”. “Data Clocks” has been set to 25 to allow for the 24 output bits plus the one additional cycle specified by the data sheet. The total number of clocks is simply the sum of these two values, in this case 32.

The “Polarity” has been set to rising edge to match the ADS1251 timing diagram. The “Frequency” has been set to 1MHz (frequency has to be high enough to ensure that 25 cycles of SCLK can be completed before the next sample is ready, the sample rate being the master clock of the ADS1251 divided by 384).

Note: The above parameters should be adjusted as needed to suit the particular values of ADS1251 master clock rate and SCLK rate demanded by the application. The “Note” field in the editor can be used to add comments describing the particular configuration and the file can be saved with a new “Display Name” and filename by using the “Save As” button.

In the next box “Data Size” is set to 24 bits and the “Data Format” is 2’s complement – both characteristics of the ADS1251. By specifying the min and max sample rate Quickfilter Pro will check the sample rate of any filters you specify to ensure they fall within the range the ADS1251 can handle.

In the upper right Quickfilter Pro has generated the necessary interconnect schematic to connect the ADS1251 to J3 on the development board, based on the specified control signals. DOUT from the ADS1251 is connected to DIN and DRDY on J3. The only other necessary connection is SCLK. Two of the signals shown are *not* required – the development board will always output filtered data on the DOUT pin (which could be used if an external host controller is also connected) and the CS signal is required only for the QF1D512(s) on the development board.

3) Configuration Files

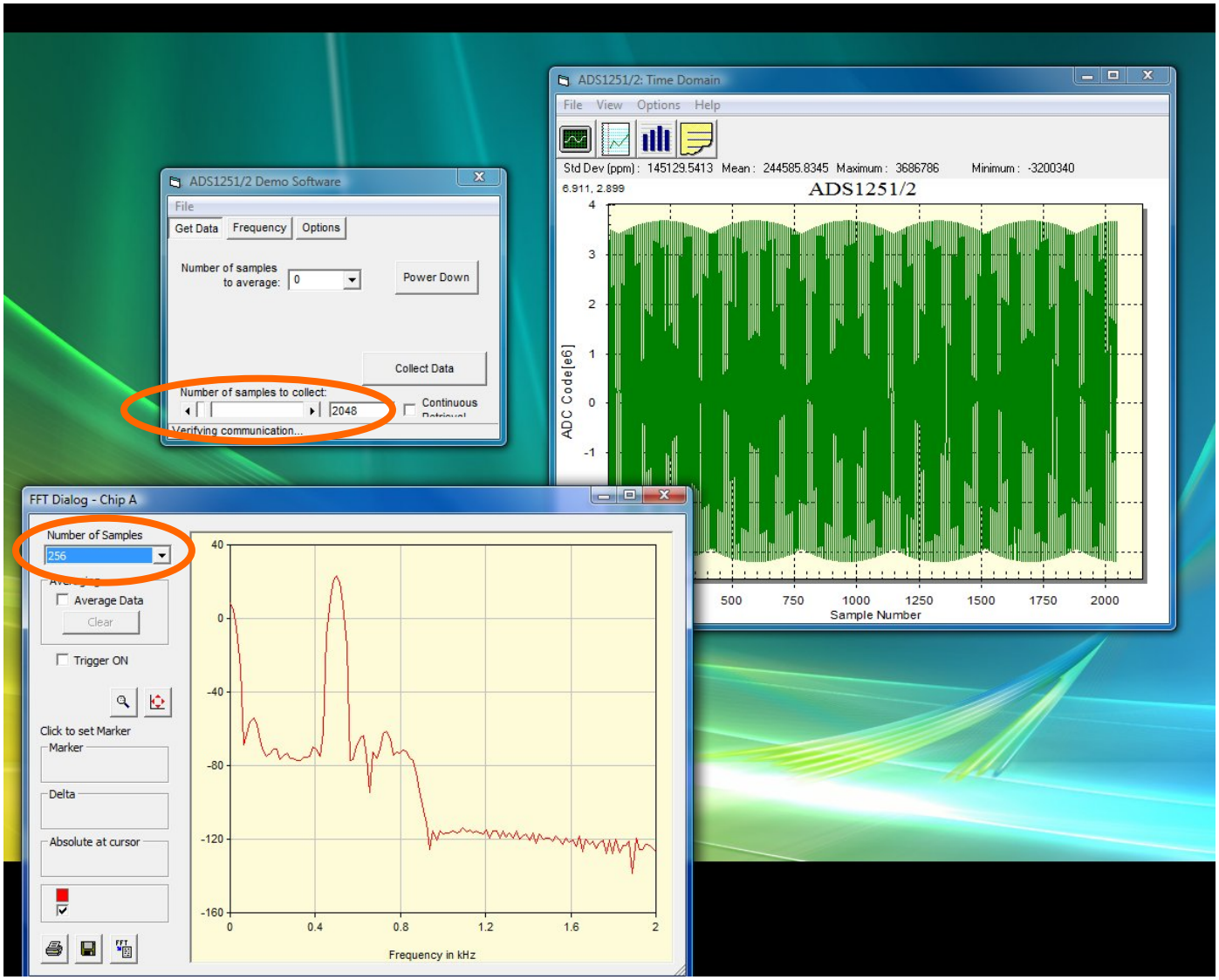
The configuration file provided (**ADS1251.q1d2**) is quite straightforward. There are no header bits in the output data stream so the header length is set to zero, as is the data offset. The data length is 24 bits and the data format is 2’s complement. In the Pin Settings editor the only key parameters are DCLK polarity – rising edge (DCLK for the QF1D512 is driven by the SCLK signal) and DSEL active low to match the CS signal we generated in the Input Source Editor.

Note: The sampling rate of this file should be modified as needed to match the sampling rate in use for the ADS1251. The filter characteristics may also be modified as needed. The sample rate and filter response can be modified by clicking on Edit in the main configuration window.

4) Using the TI ADS1251 EVM board

When using the ADS1251 EVM an on-board controller and oscillator provide the necessary timing and control signals. Supplied software can be used to set up the user’s desired sample rate. Interface to the QF1D512-DK consists of just two lines which are conveniently available from jumper sites on the EVM., SCLK appears on J4 of the EVM board and DOUT/DRDY on J5. It is not necessary to break the hardwired links across the jumper pins on the board. Since SCLK is externally generated use **ADS1251ext.adc** as the Input Signal Source file. The controller on the EVM causes data collection to happen in “bursts” according to the number of samples specified in the software. This number should be set higher than the “number of samples” specified in the Quickfilter Pro FFT window for best results. (since there is no

convenient way of syncing the start of a data collection cycle there is a greater probability of collecting a complete sequence of samples in Quickfilter Pro if the TI software is set to sample a much greater number of samples). The following screenshot illustrates the TI software set to collect 2048 samples, whereas the Quickfilter Pro FFT Dialog is set for 256 samples:



Another way to use the ADS1251 is to break the links connecting DOUT/DRDY and SCLK to the EVM host controller and connecting the ADC side of these signals to the QF1D512-DK. In this scenario the EVM controller simply provides the master clock to the ADC, all control signals are generated by the QF1D512-DK. In this mode use the **ADS1251dk.adc** Data Input Source file and follow the instructions in Section 2.

5) Additional Notes

The provided file, ADAS1251DK.adc, and the comments in Section 2 assume a standalone ADS1251 connected to the development board. If it is desired to insert the QF1D512s on the development board in series between the ADS1251 and an external host controller (for example on the ADS1251 Evaluation board as described above) only a minor revision is required to the supplied file. In particular the SCLK signal will now be generated externally by the host controller. Simply change the source of SCLK in the dropdown in the Input Source Editor. An input source file incorporating this change, **ADS1251ext.adc**, is available for download. The DOUT pin on J3 returns filtered data to the host controller.

Note: Please ensure that you do not specify SCLK as an output from the QF1D512-DK when you are supplying an externally generated SCLK signal!

Other considerations when using the QF1D512 in the user's application:

As detailed above the development board uses the FPGA to generate the necessary framing signal (CS) to drive DSEL on the QF1D512. In the end application the host controller must generate this signal. The actual timing of the signal will depend on the data mode to be used - SPI normal, SPI continuous, or synchronous serial. Please refer to the QF1D512 data sheet for more information.

More detailed information on Data Input Source files and Configuration files can be found in the QF1D512-DK Users Guide. This is automatically stored on your computer when Quickfilter Pro is installed. You can find the document within the program by clicking on "Help / Open Documents Folder". Alternatively it can be downloaded from the web at http://www.quickfiltertech.com/files/QF1D512-DK%20Users%20Guide.pdf .

There is also a brief overview of the functions of these files in Application Brief QFAB001, available here: http://www.quickfiltertech.com/html/app_notes.php .

Demo Files available:

ADS1251dk.adc	Data Input Source file for DK generated SCLK
ADS1251ext.adc	Data Input Source file for externally generated SCLK
ADS1251.q1d2	Example configuration file

Other links of interest:

QF1D512-DK Product Page:	http://www.quickfiltertech.com/html/qfilter_page.php?content_id=55
Input Signal Source Files:	http://www.quickfiltertech.com/html/qfilter_page.php?content_id=66
ADS1251 Product Page:	http://focus.ti.com/docs/prod/folders/print/ads1251.html
ADS1251 Data Sheet:	http://www.ti.com/lit/gpn/ads1251
ADS1251EVM Demo Board:	http://www.ti.com/litv/pdf/sbau041

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